



**A low cost  
CMOS 500Mbyte/sec  
SCI link controller**

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### ❑ **LC-2 Functional Description and High Level Block Diagram**

- Motivations
- Overview
- Application Example
- Simplified Block Diagram
- Sample Packet Traversal
- Dolphin SCI Interface Migration

### ❑ **LC-2 Design Methods and Tools**

- Tools
- Simulation Environment
- Other Dolphin ASIC Designs

## Motivations for LC-2

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### ❑ High Performance

- 500 Mbytes/sec per link
- 2.5 times previous generation
- Reduced latency

### ❑ Low Cost for PC Server Interfaces

- Target less than \$50
- Avoid exotic semiconductor technologies & multiple supply voltages
- Limit pin count to utilize acceptable packaging

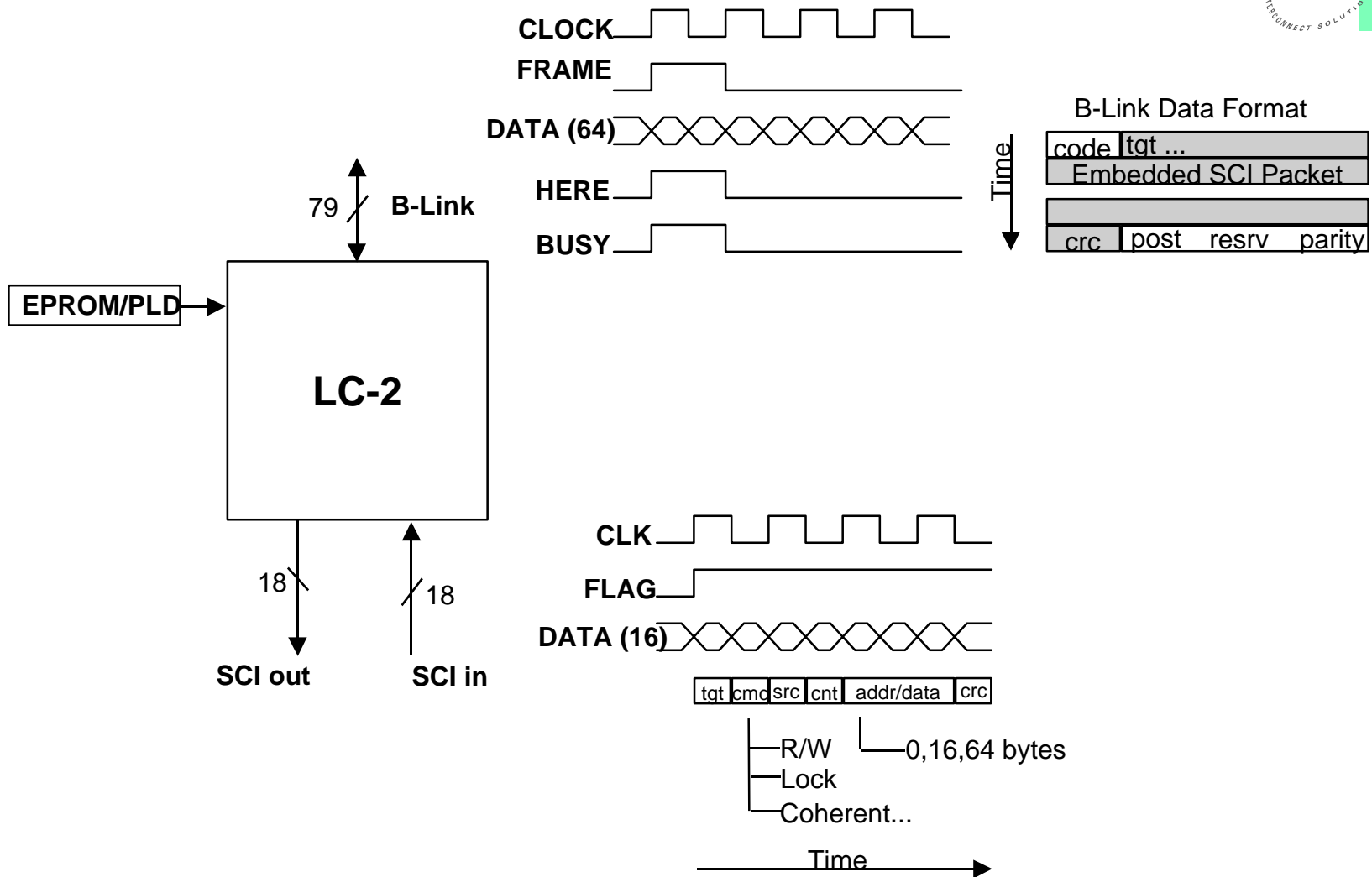
### ❑ Low Power

- Target - 2W
- Avoid special cooling

### ❑ Time to Market

➤ **CMOS and Standard ASIC Tools**

# LinkController-2 Overview





### ❑ **SCI links**

- IEEE SCI Std. 1596-1992 Protocols
- IEEE SCI 1596.3-1996 Low Voltage Differential Signaling (LVDS)

### ❑ **B-Link**

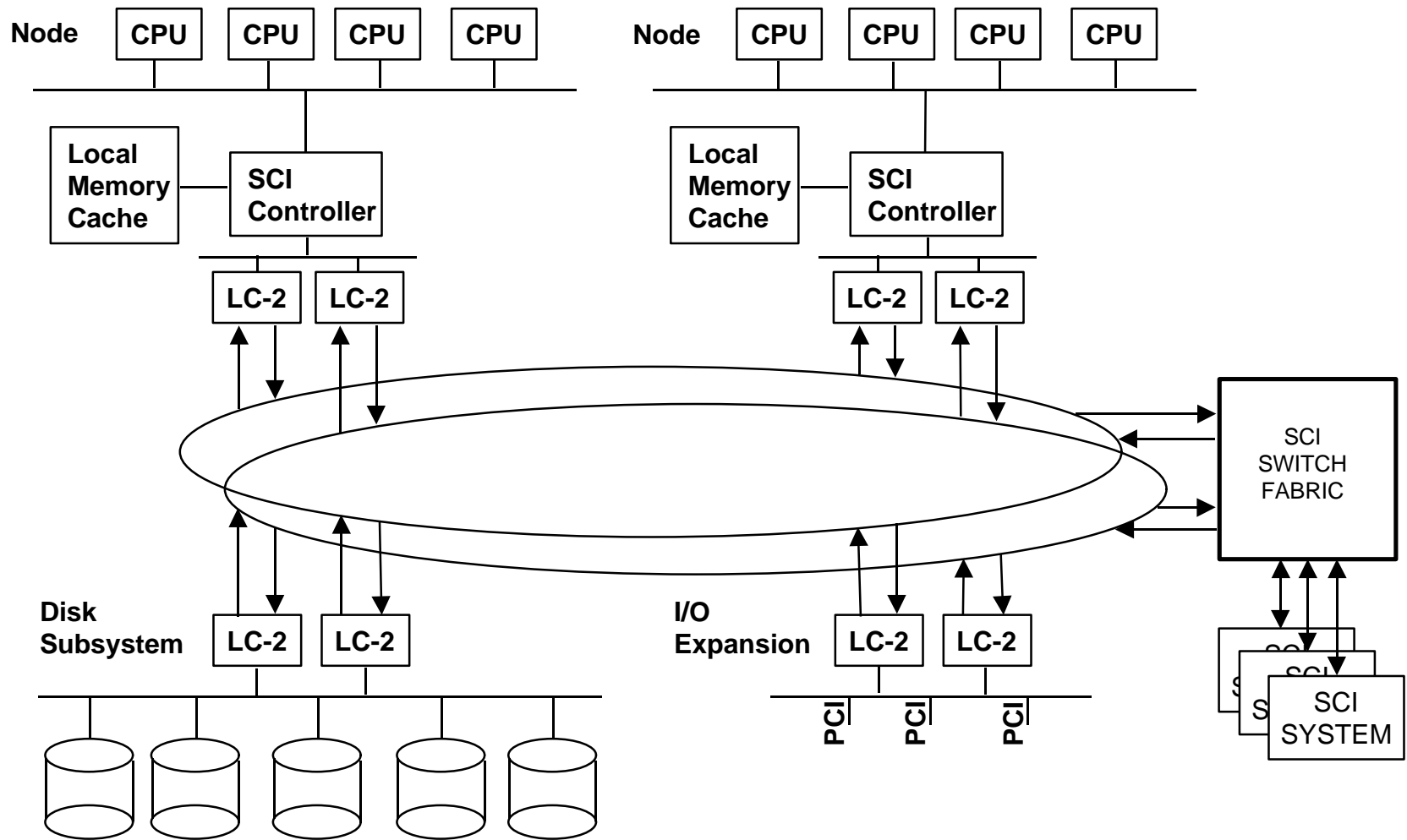
- Low Signal Count
  - ◆ Packet Transfer Format
  - ◆ Embedded SCI Packets (multiplexed address/data)
- Multi Master Bus Arbitration
  - ◆ General Purpose
  - ◆ Redundant Links
  - ◆ Interleaving
- Split Transaction
  - ◆ High Performance
  - ◆ Compliant with SCI
  - ◆ Enables Pipelining (multiple outstanding transactions)



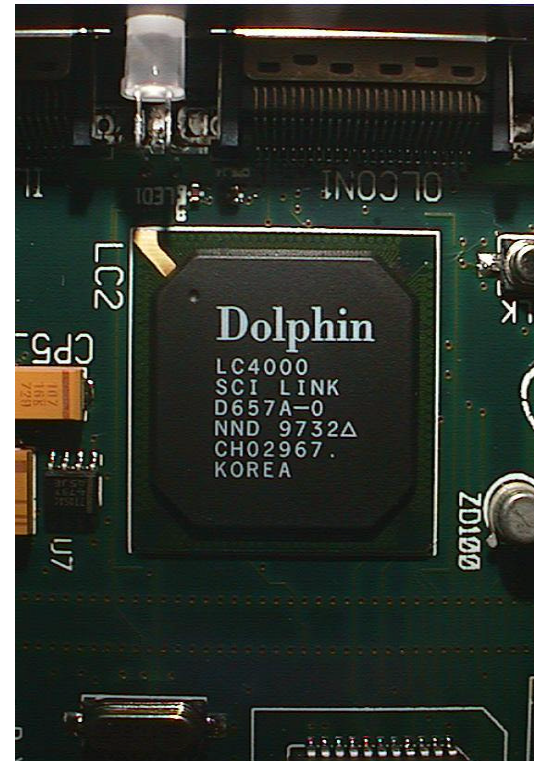
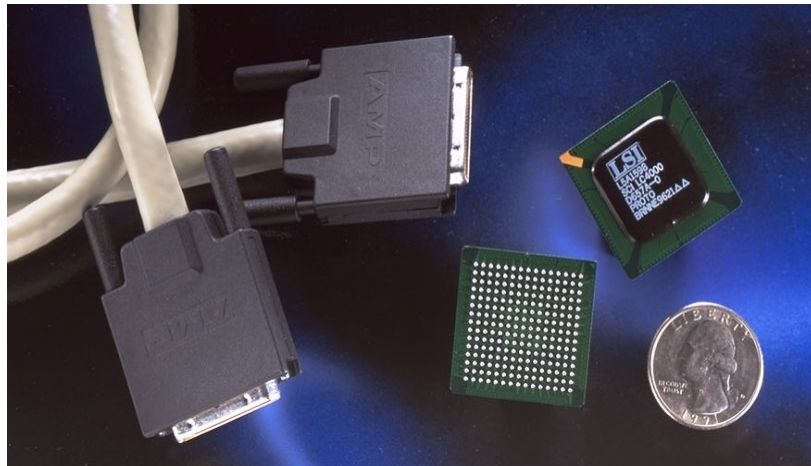
### □ Core Functionality

- 32-bit Link Pipeline
  - ◆ 32-bit Parallel CRC-16 Calculation in single cycle
- Flexible Packet Switch Routing
  - ◆ Two 256x1 RAM blocks table routing
  - ◆ Interval routing using mask and compare of targetid/nodeid
- 4 Transmit & 4 Receive Dynamic Queues
  - ◆ Capable of storing 3 req/3 res in each direction
- Hardware Initialization
  - ◆ Automatic scrubber selection
  - ◆ Initial nodeid assignment
- Performance Counters
  - ◆ Will count packets received, bypassed, transmitted, etc.
  - ◆ Masked compare of command symbol
- IEEE Std 1212 Control Status Register Support
- IEEE Std 1149.1 Test Access Port

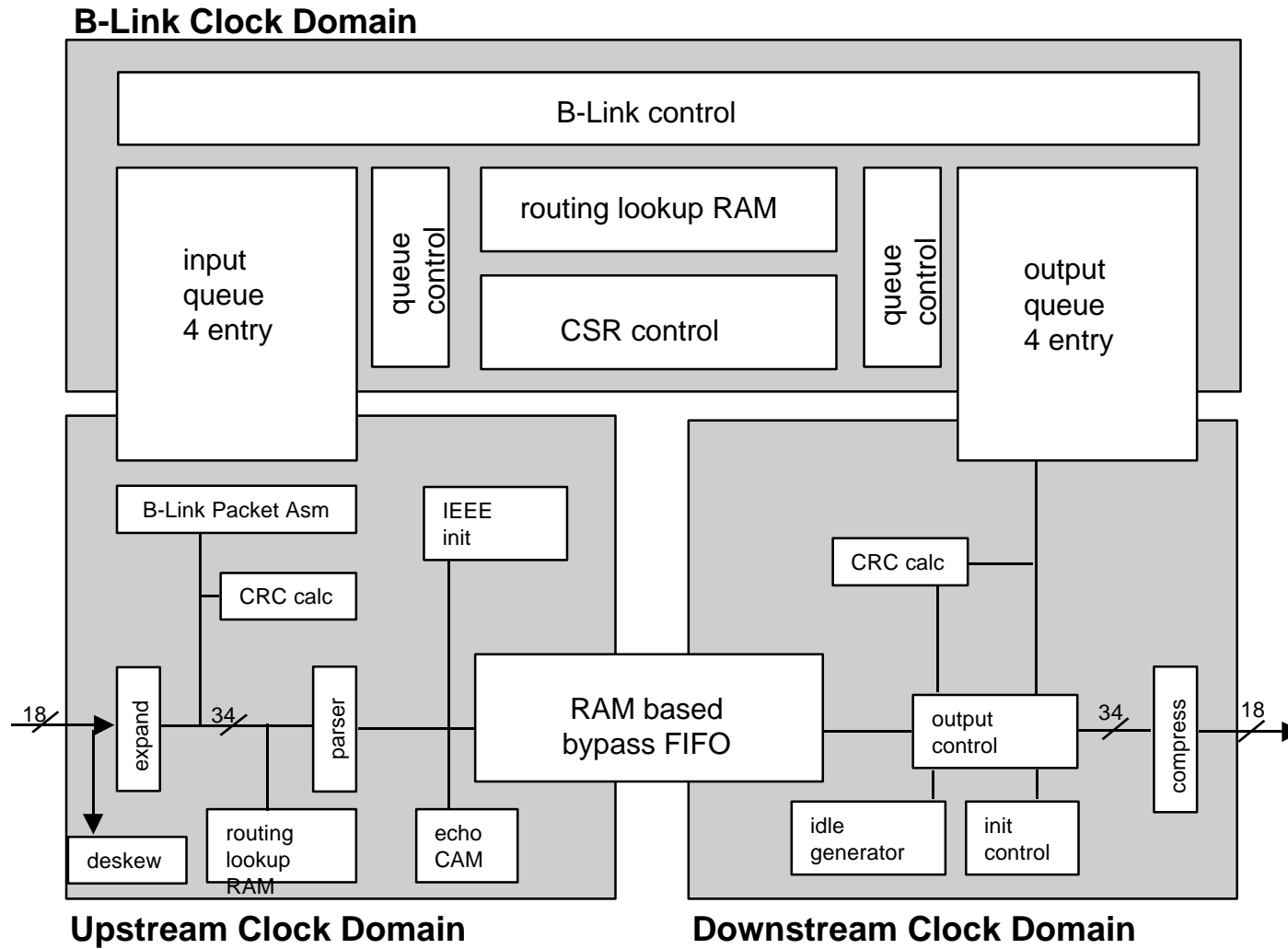
# LC-2 APPLICATION EXAMPLE



# LC-2 Photo



# LC-2 Simplified Block Diagram



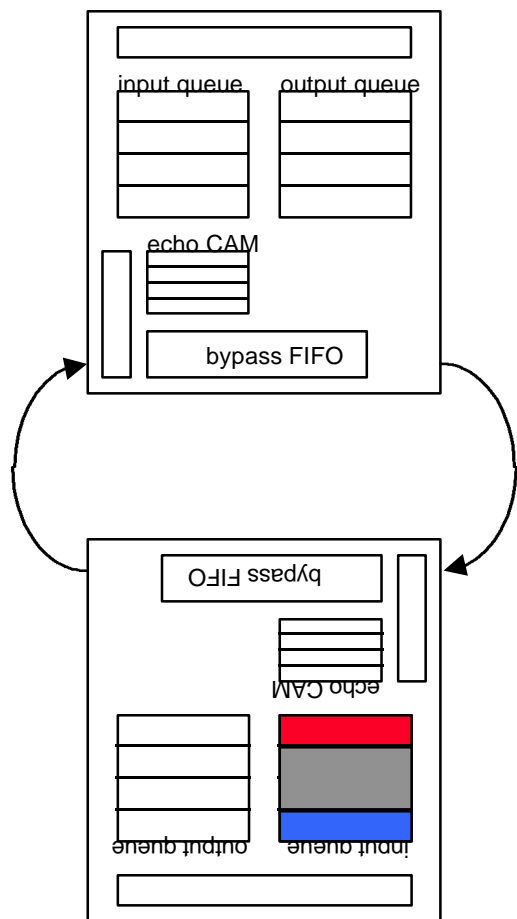
# Sample Packet Traversal



# Sample Packet Traversal (cont.)



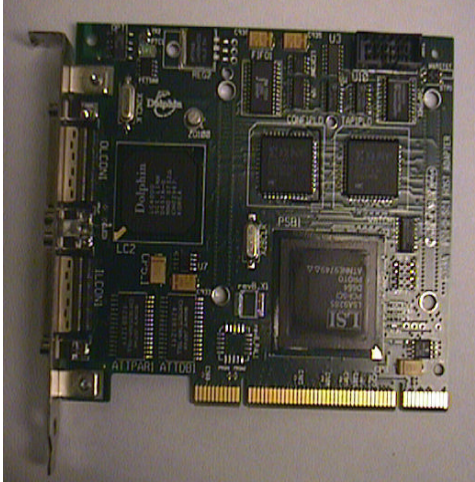
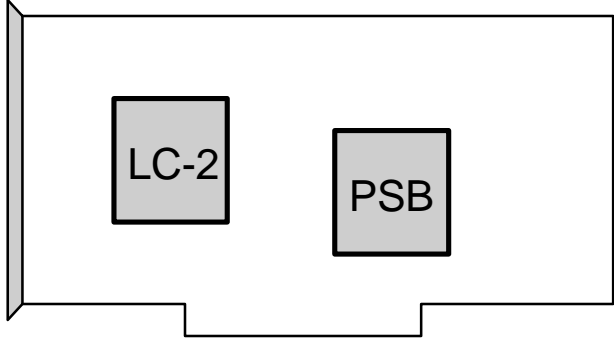
# Sample Packet Traversal (cont.)



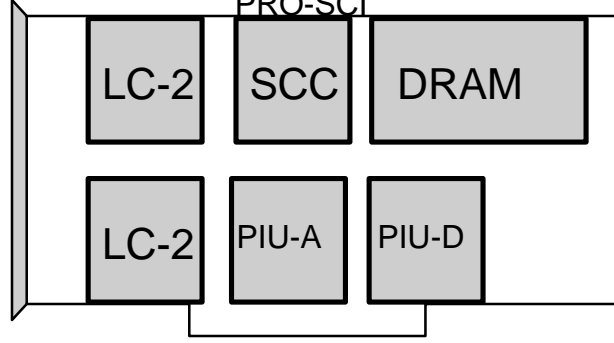
# Application Examples



Shared Nothing  
PCI-SCI



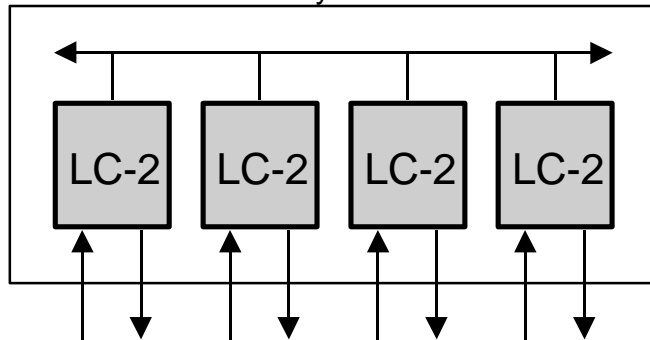
Shared Memory  
Cache Coherent  
PRO-SCI



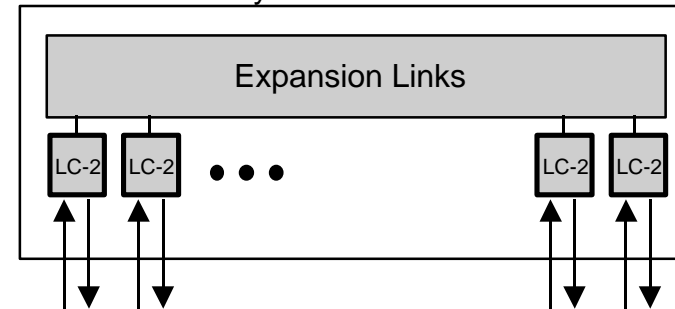
## Application Examples, cont.



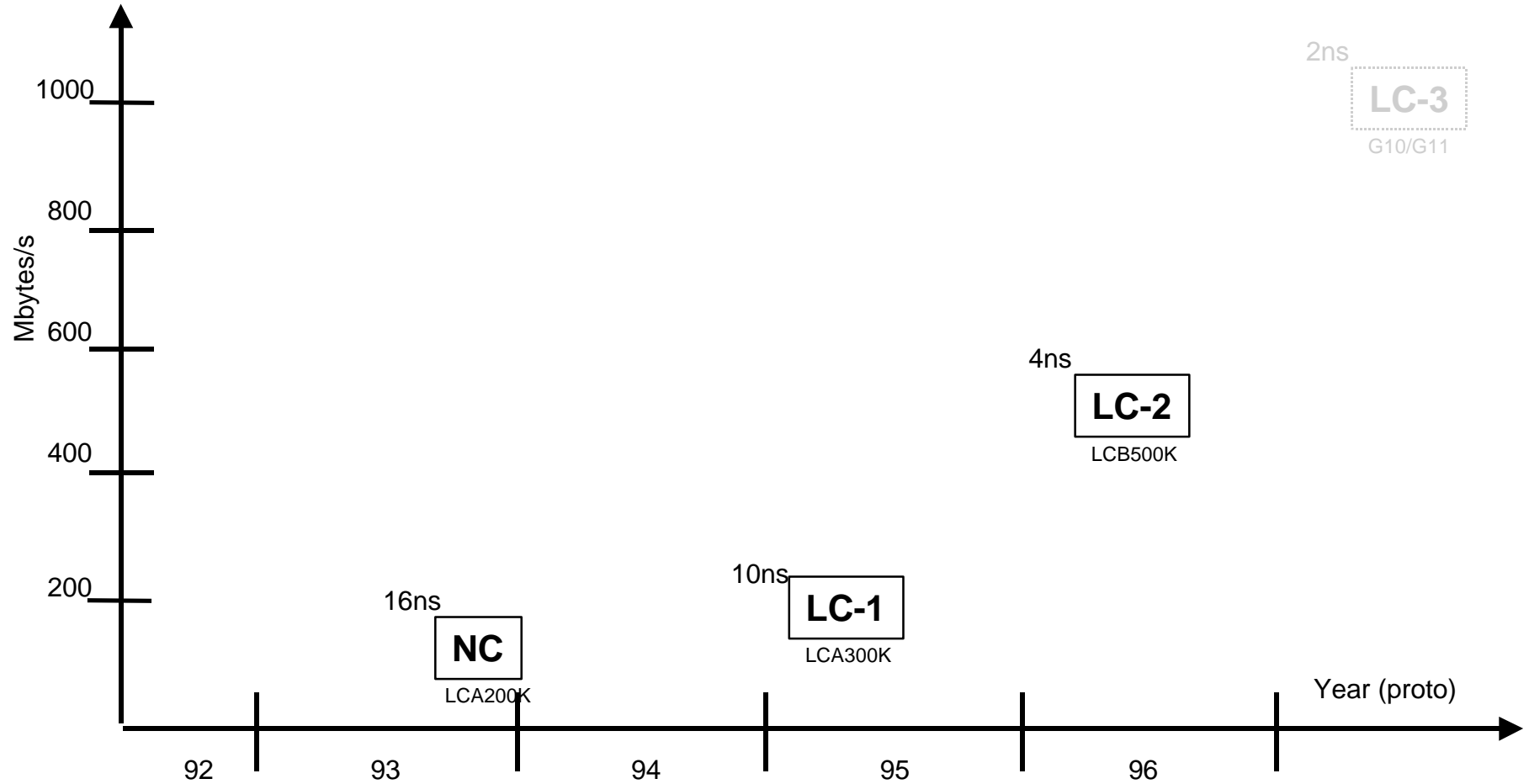
Low Cost  
4-way Switch



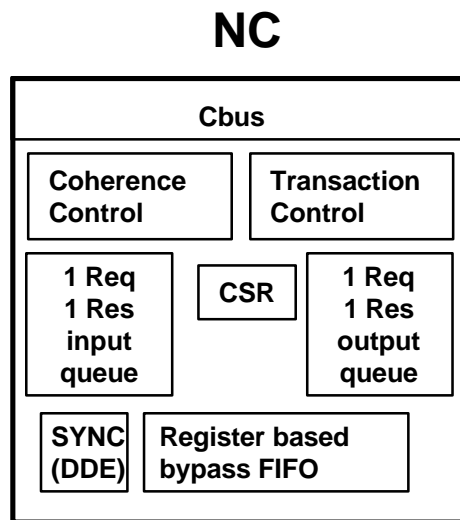
High Performance  
16-way Scalable Switch



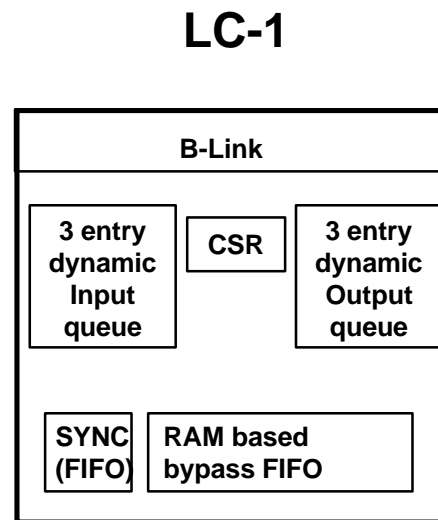
# Dolphin SCI Interface Migration



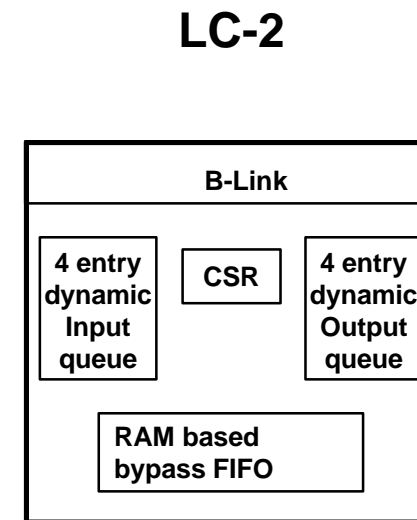
## Dolphin SCI Interface Migration (cont.)



**H-GaAs-III/LCA200K**  
 14.9x14.7 mm  
 125 MB/s @ 31.25 MHz  
 Cbus @ 31.25 MHz  
 Aprx power 5W  
 299 CPGA  
 Proto date 10/93



**LCA300K**  
 8.95 x 8.95 mm  
 200 MB/s @ 50 MHz  
 B-Link @ 50 MHz  
 Aprx power 3.5W  
 208 MQFP  
 Proto date 3/95



**LCB500K**  
 7.3 x 7.3 mm  
 500 MB/s @ 125 MHz  
 B-Link @ 100 MHz  
 Aprx power 2.5W  
 225 PBGA  
 Proto date 5/96

## Conclusion



	<i>LC-1</i>	<i>LC-2</i>
<b>Technology</b>	<b>LSI 300K CMOS</b>	<b>LSI 500K</b>
<b>CMOS</b>		
<b>Power Consumption</b>	<b>max 3.5 W</b>	<b>max 2.5 W</b>
<b>SCI Link Frequency</b>	<b>50 MHz</b>	<b>125 MHz</b>
<b>SCI Link Bandwidth</b>	<b>200 Mbytes/sec</b>	<b>500</b>
<b>Mbytes/sec</b>		
<b>B-Link Frequency</b>	<b>50 MHz</b>	<b>100 MHz</b>
<b>B-Link Bandwidth</b>	<b>500 Mbytes/sec</b>	<b>800</b>
<b>Mbytes/sec</b>		
<b>Node Bypass Latency</b>	<b>140ns</b>	<b>48ns</b>
<b>B-Link -&gt; SCI on read request</b>	<b>180ns</b>	<b>72ns</b>
<b>SCI -&gt; B-Link on read request</b>	<b>290ns</b>	<b>114ns</b>
<b>Packaging</b>	<b>208 MQFP</b>	<b>225 PBGA</b>

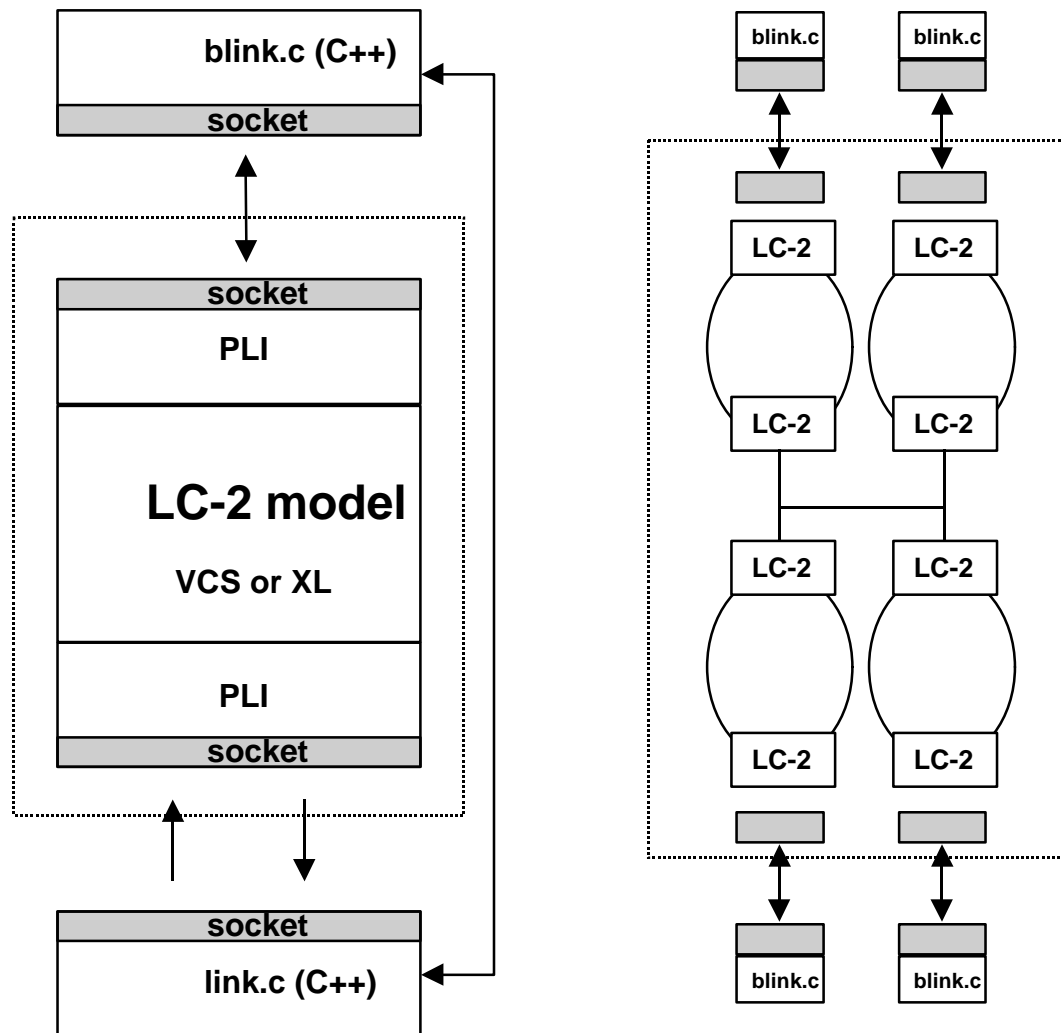


- ❑ **Source Code in Verilog RTL**
  - Cadence Verilog XL
  - Chronologic VCS
  - Dolphin Source Code Retrieval System (SCCS)
  - DAI Signalscan Waveform Viewer
- ❑ **Synthesis to Gate Level**
  - Synopsys Design Compiler Expert
- ❑ **Static Timing Analysis**
  - Motive
  - Synopsys
  - Vendor tools
- ❑ **Scan Insertion & ATPG**
  - Vendor tools
- ❑ **Floorplanning and Placement**
  - Synopsys Floorplan Manager
  - Vendor tools



### □ Functional Verification

- Chronologic VCS to simulate large topologies
  - ◆ Up to 72 instances of LC-2 simulated
- Dolphin test system
  - ◆ Topology generator
  - ◆ C++ base stimuli generators and analyzers
  - ◆ Link Class Library
  - ◆ B-Link Class Library
  - ◆ Single node tests suites
  - ◆ System simulation test suites



## Special Tests

- RAM Test
- BIST
- Functional
- JTAG Test
- Cable Skew Test
- XTAL Drift Test

## Other Dolphin ASIC Designs



Design	GaAs NodeChip	CMOS NodeChip	LC-1	PSB	LC-2	SCC
Proto Date	Mar 93	Dec 93	Mar 95	Feb 96	May 96	Dec 96
Technology	VGFX 350K	LCA 200K	LCA 300K	LEA 500K	LCB 500K	LEA 500K
Die Size	14.9x14.7mm	14.9x14.7 mm	8.95x8.95 mm	11.7x11.7mm	7.3x7.3mm	11.7x11.7mm
Package	557 PPGA	299 CPGA	208 MQFP	313 EPBGA	225 PBGA	388 EPBGA
JTAG	no	no	no	yes	yes	yes
No of RAMS	2	2	6	12	8	16
Clock Domains	3	3	3	2	3	1
Approx. Power	33.7 W	5 W	3.5 W	3.5 W	2.5 W	4 W
B-Link Frequency	31.25 (C-BUS)	31.25 (C-BUS)	50 MHz	50 MHz	100 MHz	50 MHz
Link Bandwidth	500 MB/s	125 MB/s	200 MB/s	N/A	500 MB/s	N/A



### ❑ **Dolphin & SCI Web Sites**

- <http://www.dolphinics.com> - Dolphin US
- <http://www.dolphinics.no> - Dolphin Europe
- <http://www.scizzl.com> - SCizzL - SCI LAMP Association

### ❑ **Universities and Research Institutions**

- <http://www.ifi.uio.no/~sci> - University of Oslo
- <http://www.cs.ucsb.edu/research/sci> - UCSB
- <http://www.uni-paderborn.de/fachbereich/AG/heiss/arminius> - Paderborn
- <http://www.bode.informatik.tu-muenchen.de/sci> - München
- <http://www.hcs.ufl.edu> - University of Florida
- <http://www.cern.ch/RD24> - CERN

### ❑ **Computer Vendors**

- <http://www.dg.com/numaline> - Data General
- <http://www.sun.com/servers/hpc/press/background.html> - SUN
- <http://www.scali.com> - SCALI

### ❑ **Slides at**

- <ftp://ftp.dolphinics.no/pub/pegu/ucsb0298.pdf>