

Peter Cappello
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University of California, Santa Barbara
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EDUCATION

Ph.D. Princeton University 1982

APPOINTMENTS

1994 - present	Professor	UC, Santa Barbara
1988 - 1994	Associate Professor	UC, Santa Barbara
1982 - 1988	Assistant Professor	UC, Santa Barbara

CURRENT RESEARCH INTERESTS

- Parallel and distributed computing
- Multiprocessor scheduling

PUBLICATIONS

JOURNAL ARTICLES

1. Peter R. Cappello and Kenneth Steiglitz. A VLSI Layout for a Pipelined Dadda Multiplier. *ACM Trans. on Computer Systems*, **1**(2):157–174, May 1983 (reprinted as a book chapter).
2. Peter R. Cappello and Kenneth Steiglitz. Completely Pipelined Architectures for Digital Signal Processing. *IEEE Trans. on Acoust., Speech, Signal Processing*, **31**(4):1016–1023, Aug. 1983.
3. Peter R. Cappello, Andrea LaPaugh, and Kenneth Steiglitz. Optimal Choice of Intermediate Latching to Maximize Throughput in VLSI Circuits. *IEEE Trans. on Acoust., Speech, Signal Processing*, **32**(1):28–33, Feb. 1984.
4. Peter R. Cappello and Kenneth Steiglitz. Some Complexity Issues in Digital Signal Processing. *IEEE Trans. on Acoust., Speech, Signal Processing*, **32**(5):1037–1041, Oct. 1984.
5. Peter R. Cappello and Kenneth Steiglitz. Unifying VLSI Array Design with Linear Transformations of Space-Time. In Franco P. Preparata, editor, *Advances in Computing Research*, vol. 2: VLSI Theory, pages 23–65, JAI Press, Inc., Greenwich, CT, 1984.
6. Peter R. Cappello and Kenneth Steiglitz. A Note on Free Accumulation in VLSI Filter Architectures. *IEEE Trans. on Circuits Syst.*, **CAS-32**(3):291–296, Mar. 1985.
7. Peter R. Cappello. Gaussian Elimination on a Hypercube Automaton. *J. Parallel and Distributed Computing*, **4**(3):288–308, June 1987.
8. Peter R. Cappello and Cheng-Wen Wu. Computer-Aided Design of VLSI FIR Filters. *Proc. IEEE*, **75**(9):1260–1271, Sep. 1987 (also translated into Russian).

9. Cheng-Wen Wu and Peter R. Cappello. Application-Specific CAD of VLSI Second-Order Sections. *IEEE Trans. Acoust., Speech, Signal Processing*, **36**(5):813–825, May 1988.
10. Peter R. Cappello and Alan J. Laub. Systolic Computation of Multivariable Frequency Response. *IEEE Trans. Autom. Control*, **33**(6):550–558, June 1988.
11. Peter R. Cappello and Willard L. Miranker. Systolic Super Summation. *IEEE Trans. Comput.*, **37**(6):657–677, June 1988.
12. Grant Davidson, Peter R. Cappello, and Allen Gersho. Systolic Architecture for Vector Quantization. *IEEE Trans. Acoust., Speech, Signal Processing*, **36**(10):1651–1664, Oct. 1988 (reprinted as a book chapter).
13. Cheng-Wen Wu and Peter R. Cappello. Block Multipliers Unify Bit-Level Cellular Multiplication. *Intl. J. Computer Aided VLSI Design*, **1**(1):113–125, July 1989.
14. Bradley R. Engstrom and Peter R. Cappello. The SDEF Programming System. *J. Parallel and Distributed Computing*, **7**:201–231, 1989.
15. Yoav Yaacoby and Peter R. Cappello. Scheduling a System of Nonsingular Affine Recurrence Equations onto a Processor Array. *J. VLSI Signal Processing*, **1**(2):115–125, 1989.
16. Cheng-Wen Wu and Peter R. Cappello. Easily Testable Iterative Logic Arrays. *IEEE Trans. Comput.*, **39**(5):640–652, May 1990.
17. Peter R. Cappello, Efstratios Gallopoulos, and Cetin K. Koc. Systolic Computation of Interpolating Polynomials. *Computing*, **45**:95–118, 1990.
18. Cetin K. Koc, Peter R. Cappello, and Efstratios Gallopoulos. Decomposing Polynomial Interpolation for Systolic Arrays. *Int. J. Computer Mathematics*, **38**:219–239, 1991.
19. Peter R. Cappello. A Processor-Time-Minimal Systolic Array for Cubical Mesh Algorithms. *IEEE Trans. Parallel and Distributed Systems*, **3**(1):4–13, Jan. 1992.
20. Peter R. Cappello and Willard L. Miranker. Systolic Super Summation with Reduced Hardware. *IEEE Trans. Comput.*, **41**(3):339–342, March 1992.
21. Chris J. Scheiman and Peter R. Cappello. A Processor-Time-Minimal Systolic Array for Transitive Closure. *IEEE Trans. on Parallel and Distributed Systems*, **3**(3):257–269, May 1992.
22. Yoav Yaacoby and Peter R. Cappello. Decoupling the Dimensions of a System of Affine Recurrence Relations. *Linear Algebra and Its Applications*, **167**:157–170, April 1992.
23. Cetin K. Koc and Peter Cappello. Systolic Arrays for Integer Chinese Remaindering. *Parallel Computing*, **19**:1303–1311, 1993.
24. Chris J. Scheiman and Peter Cappello. A Period-Processor-Time-Minimal Schedule for Cubical Mesh Algorithms. *IEEE Trans. on Parallel and Distributed Systems*, **5**(3): 274 – 280, Mar. 1994.
25. Yoav Yaacoby and Peter Cappello. Bounded Broadcast in Systolic Arrays. *Int. J. of High Speed Computing*, **6**(2):223-237, 1994.
26. John Bruno and Peter R. Cappello. Implementing the 3D Alternating Direction Method on the Hypercube. *J. Parallel and Distributed Computing*, **23**:411–417, 1994.

27. Yoav Yaacoby and Peter Cappello. Converting Affine Recurrence Equations to Quasi-Uniform Recurrence Equations. Magdy Bayoumi, Editor, *J. of VLSI Signal Processing*, **11**:1 & 2, pp. 113-131, Oct. 1995.
28. Chris J. Scheiman and Peter Cappello. A Processor-Time-Minimal Schedule for 3D Rectilinear Mesh Algorithms. *Parallel Processing Letters*, **6**(4):539-550, Dec. 1996.
29. Bernd O. Christiansen, Peter Cappello, Mihai F. Ionescu, Michael O. Neary, Klaus E. Schauser, and Daniel Wu. Javelin: Internet-Based Parallel Computing Using Java. *Concurrency: Practice and Experience*, **9**(11): 1139 - 1160, Nov. 1997.
30. Peter Cappello and Omer Egecioglu. Processor Lower Bound Formulas for Array Computations and Parametric Diophantine Systems. *International Journal of Foundations of Computer Science*, **9**(4):351-375, 1998, World Scientific Publishing Company. Accepted for publication 20 November 1997.
31. M. O. Neary, B. O. Christiansen, P. Cappello, and K. E. Schauser. Javelin: Parallel computing on the internet. *Future Generation Computer Systems*, Elsevier Science, Amsterdam, Netherlands, **15**(5-6):659-674, October 1999.
32. M. O. Neary, S. P. Brydon, P. Kmiec, S. Rollins, and P. Cappello. Javelin++: Scalability Issues in Global Computing. *Concurrency: Practice and Experience*, **12**:727 - 753, 2000. (Received 1 Aug 99. Revised 15 Nov 99. Accepted Nov 99.)
33. Peter Cappello, Omer Egecioglu, and Chris Scheiman. Processor-time-optimal systolic arrays. *Parallel Algorithms and Applications*, **15**:167 - 199, 2000.
34. Peter Cappello and Dimitrios Mourloukos. CX: A Scalable, Robust Network for Parallel Computing. **10**(2): 159 - 171, *Scientific Programming Journal* (Special Issue on Grid Computing, Ewa Deelman and Carl Kesselman, eds.), 2002. (<http://iospress.metapress.com/link.asp?id=mwq0y3utf3nq>)
35. Michael O. Neary and Peter Cappello. Advanced Eager Scheduling for Java-Based Adaptively Parallel Computing. *Concurrency and Computation: Practice and Experience*, **17**:797 - 819, 2005. Published online in Wiley Interscience (www.interscience.wiley.com). DOI: 10.1002/cpe.855.
36. Peter Cappello. Application-Specific Processor Architecture: Then, Now, and Beyond. *Submitted, J. VLSI Signal Processing*, 2007.

CONFERENCE PAPERS

1. Peter R. Cappello and Kenneth Steiglitz. Some Intractable Problems in Digital Signal Processing. In *Proc. IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pages 43–46, Atlanta, Mar. 1981.
2. Peter R. Cappello and Kenneth Steiglitz. Digital Signal Processing Applications of Systolic Algorithms. In *Proc. CMU Conference on VLSI Systems & Computations*, Pittsburgh. Published as *VLSI Systems & Computations*, H.-T. Kung, R. Sproul, and Guy Steele, editors, pages 245–254, Computer Science Press Rockville, MD, Oct. 1981.
3. Peter R. Cappello and Kenneth Steiglitz. Bit-Level Fixed-Flow Architectures for Signal Processing. In *Proc. IEEE Int. Conf. on Circuits and Computers*, pages 570–573, New York, Sep. 1982.
4. Peter R. Cappello, Andrea LaPaugh, and Kenneth Steiglitz. Optimal Choice of Intermediate Latching to Maximize Throughput in VLSI Circuits. In *Proc. IEEE Int. Conf. on Acoustic, Speech, and Signal Processing*, pages 935–938, Boston, Apr. 1983.

5. Peter R. Cappello and Kenneth Steiglitz. Unifying VLSI Array Design with Geometric Transformations. In *Proc. Int. Conf. on Parallel Processing*, pages 448–457, Bellaire, MI, Aug. 1983 (reprinted as a book chapter).
6. Peter R. Cappello and Kenneth Steiglitz. A Fast Tally Structure and Applications to Signal Processing. In *Proc. Int. Conf. on Acoustics, Speech, and Signal Processing*, San Diego, Mar. 1984.
7. (Invited) Peter R. Cappello and Kenneth Steiglitz. Selecting Systolic Designs Using Linear Transformations of Space-Time. In *Proc. SPIE Conference: Real-Time Signal Processing VII*, Vol. 495, pages 75–85, San Diego, Aug. 1984.
8. Peter R. Cappello. Towards an FIR Filter Tissue. In *Proc. Int. Conf. on Acoustics, Speech, and Signal Processing*, pages 276–279, Tampa, FL, Mar. 1985.
9. Peter R. Cappello. A Mesh Automaton for Solving Dense Linear Systems. In *Proc. Int. Conf. on Parallel Processing*, pages 418–425, St. Charles, IL, Aug. 1985.
10. (Invited) Peter R. Cappello. Transforming Systolic Arrays in Spacetime. Int. Workshop on Digital Communications. Tirrenia, ITALY, Sep. 1985. Published as *Digital Communications*, Ezio Biglieri and Giancarlo Prati, editors, pages 219–233, North-Holland, New York 1986.
11. (Invited) Cheng-Wen Wu, and Peter R. Cappello, and Michael Saboff. An FIR Filter Tissue. In *Proc. 19th Asilomar Conf. on Circuits, Systems, and Computers*, pages 283–287, Pacific Grove, CA, Nov. 1985.
12. Peter R. Cappello, Grant Davidson, Allen Gersho, Cetin K. Koc, and V. Somayazulu. A Systolic Vector Quantization Processor for Real Time Speech Coding. In *Proc. IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pages 2143–2146, Tokyo, JAPAN, Apr. 1986.
13. (Invited) Cheng-Wen Wu and Peter R. Cappello. Application-Specific CAD of High-Throughput IIR Filters. In *Proc. 32nd IEEE Computer Society Int. Conf. (Compcon)*, pages 302–305, San Francisco, Feb. 1987.
14. Cheng-Wen Wu and Peter R. Cappello. Computer-Aided Design of VLSI Second-Order Sections. In *Proc. Int. Conf. Acoustics, Speech, and Signal Processing*, pages 44.4.1–44.4.4, Dallas, Apr. 1987.
15. Bradley R. Engstrom and Peter R. Cappello. The SDEF Systolic Programming System. In *Proc. Int. Conf. on Parallel Processing*, pages 645–652, St. Charles, IL, Aug. 1987.
16. (Invited) Bradley R. Engstrom and Peter R. Cappello. The SDEF Systolic Programming System. Princeton Workshop on Algorithm, Architecture, and Technology Issues in Models of Concurrent Computation, Princeton, Sep. 1987. Published as *Concurrent Computations*, S. K. Tewksbury, Bradley W. Dickinson, and S. C. Schwartz, editors, pages 263–301, Plenum Press, New York, 1988.
17. John Bruno and Peter R. Cappello. Implementing the Beam and Warming Method on the Hypercube. In *Proc. 3rd Conf. on Hypercube Concurrent Computers and Applications*, Vol. II (Applications), pages 1073–1087, ACM Press, Pasadena, Jan. 1988.
18. (Invited) Peter R. Cappello and Alan J. Laub. Systolic Computation of Multivariable Frequency Response. In *Proc. O-E/LASE'88 (Optoelectronics and Laser Applications in Science and Engineering) - High Speed Computing*, Vol. 880, pages 150–157, Los Angeles, Jan. 1988.

19. Yoav Yaacoby and Peter R. Cappello. Scheduling a System of Affine Recurrence Equations onto a Systolic Array. In *Proc. Int. Conf. on Systolic Arrays*, Keith Bromley, Sun-Yuan Kung, and Earl Swartzlander, editors, pages 373–382, Computer Society Press, San Diego, May 1988.
20. Yoav Yaacoby and Peter R. Cappello. Converting Affine Recurrence Equations to Quasi-Uniform Recurrence Equations. *Proc. 3rd Aegean Workshop on Computing Corfu, Greece, June, 1988*. Published as *VLSI Algorithms and Architectures*, John H. Reif, editor, pages 319–328, Springer-Verlag, June, 1988.
21. Peter R. Cappello. A spacetime-minimal systolic array for matrix product. *Proc. Int. Conf. on Systolic Arrays*, Killarney, IRELAND, May 1989. Published as *Systolic Array Processors*, John McCanny, John McWhirter, and Earl Swartzlander, Jr., editors, pages 347–356, Prentice-Hall, New York, 1989.
22. Cetin K. Koc and Peter R. Cappello. Systolic arrays for integer Chinese remaindering. In *Proc. 9th Symp. on Computer Arithmetic*, Milos D. Ercegovac and Earl Swartzlander, editors, pages 216–223, IEEE Computer Society Press, Santa Monica, Sep. 1989.
23. Chris Scheiman and Peter R. Cappello. A processor-time minimal systolic array for transitive closure. In *Proc. Int. Conf. on Application Specific Array Processors*, Sun-Yuan Kung, Earl E. Swartzlander, Jr., Jos A. B. Fortes, and K. Wojtek Przytula, editors, pages 19–30, IEEE Computer Society Press, Princeton, Sep. 1990.
24. Peter R. Cappello and Sanjay Rajopadhye. Cost measures for VLSI array design. In *Proc. IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing*, Victoria, BC, CANADA, May, 1991.
25. Chris Scheiman and Peter Cappello. A period-processor-time-minimal systolic array for cubical mesh algorithms. In *Proc. 3rd IEEE Symp. on Parallel and Distributed Processing*, Dallas, Dec. 1991.
26. Chris Scheiman and Peter Cappello. A period-processor-time-minimal schedule for cubical mesh algorithms. In *Proc. Int. Conf. on Application Specific Array Processors*, pages 261–272, Venice, ITALY, Oct. 1993. (The definition of *period* in this paper is different from that used in the 1991 IEEE SPDP conference paper, necessitating different lower and upper bounds, different proofs, etc., for the schedule.)
27. Chris Scheiman and Peter Cappello. A Processor-Time-Minimal Schedule for the Standard Tensor Product Algorithm. In *Proc. Int. Conf. on Application Specific Array Processors*, pp. 176–187, San Francisco, Aug. 1994.
28. Chris Scheiman and Peter Cappello. A Processor-Time-Minimal Systolic Array for the 3D Rectilinear Mesh. In *Proc. Int. Conf. on Application Specific Array Processors*, pages 26–33, Universite Louis Pasteur, Strasbourg, FRANCE, July 1995.
29. Fiona Gaston and Peter Cappello. Self-Esteem: The Keystone of Learning? In *Proc. Frontiers in Education*, Salt Lake City, Utah, November 6-9, 1996.
30. Peter Cappello, Bernd Christiansen, Mihai F. Ionescu, Michael O. Neary, Klaus Schauer, and Daniel Wu. Javelin: Internet-Based Parallel Computing Using Java. In *ACM Workshop on Java for Science and Engineering Computation*, 1997.
31. Peter Cappello, Bernd Christiansen, Michael O. Neary, and Klaus E. Schauer. Market-Based Massively Parallel Internet Computing. In *Proc. Third Working Conf. on Massively Parallel Programming Models*, pages 118 - 129, London, UK, Nov. 1997.

32. Peter Cappello and Omer Egecioglu. Processor Lower Bound Formulas for Array Computations and Parametric Diophantine Systems. In *Proc. International Parallel Processing Symposium and Symposium on Parallel and Distributed Processing*, pages 105 - 109, Orlando, FL, Mar 1998.
33. Michael O. Neary, Sean P. Brydon, Paul Kmiec, Sami Rollins, Peter Cappello. Javelin++: Scalability Issues in Global Computing. In *Proc. ACM Java Grande Conference*, pages 171 - 180, San Francisco, June 12-14, 1999.
34. Michael O. Neary and Peter Cappello. Internet-Based TSP Computation with Javelin. In *Proc. ICPP Workshops (Scalable Web Services)*, pp. 137 - 144, Toronto, CANADA, August 21 - 24, 2000.
35. Michael O. Neary, Alan Phipps, Steven Richman, and Peter Cappello. Javelin 2.0: Java-Based Parallel Computing on the Internet. In *Proc. Euro-Par 2000*. Munich, GERMANY, August 28 - September 1, 2000.
36. Peter Cappello and Dimitrios Mourloukos. A Scalable, Robust Network for Parallel Computing. In *Proc. Joint ACM Java Grande - ISCOPE (Int. Symp. on Computing in Object-Oriented Parallel Environments)*, pages 78 - 86, Stanford University, June 2 - 4, 2001.
37. Peter Cappello and Omer Egecioglu. Automatic Processor Lower Bound Formulas for Array Computations. In *Proc. Int. Symp. Parallel Architectures, Algorithms and Networks (ISPAN)*, pages 59-64, Metro Manila, Philippines, May 2002.
38. Michael O. Neary and Peter Cappello. Advanced Eager Scheduling for Java-Based Adaptively Parallel Computing. In *Proc. Joint ACM Java Grande - ISCOPE (Int. Symp. on Computing in Object-Oriented Parallel Environments)*, pages 56 - 65, Seattle, Nov, 2002.
39. Peter Cappello. Janet's Abstract Distributed Service Component. In *Proc. 15th IASTED Int. Conf. on Parallel and Distributed Computing and Systems*, pages 751 - 756, Marina del Rey, CA, Nov. 2003.
40. Peter Cappello and Christopher James Coakley. Jicos: A Java-Centric Network Computing Service. In *Proc. 17th IASTED Int. Conf. Parallel and Distributed Computation and Systems (PDCS)*, S.Q. Zheng (ed.), pp. 510 - 515. Phoenix, AZ, Nov. 2005.

EDITED BOOK

Peter R. Cappello et al., editors. *VLSI Signal Processing*, IEEE Press, Inc., New York, 1984.

BOOK CHAPTERS

1. Peter R. Cappello and Kenneth Steiglitz. Unifying VLSI Array Design with Linear Transformations of Space-Time. In Franco P. Preparata, editor, *Advances in Computing Research*, vol. 2: VLSI Theory, pages 23-65, JAI Press, Inc., Greenwich, CT, 1984.
2. Peter R. Cappello and Kenneth Steiglitz. Unifying VLSI Array Design with Geometric Transformations. In *Tutorial: Interconnection Networks for Parallel and Distributed Processing*, C. Wu and Tse-yun Feng, editors, IEEE Computer Society Press, Aug. 1984 (reprinted conference article).
3. Peter R. Cappello. Spacetime Transformations of Cellular Algorithms. In *Systolic Signal Processing Systems*, Earl E. Swartzlander, Jr., editor, pages 161-207, Marcel Dekker Inc., New York, NY., July 1987.

4. Peter R. Cappello and Kenneth Steiglitz. A VLSI Layout for a Pipelined Dadda Multiplier. In *Computer Arithmetic, II*, Earl E. Swartzlander, Jr., editor, pages 205–222, IEEE Computer Society Press, 1990, (reprinted journal article).
5. Grant Davidson, Peter R. Cappello, and Allen Gersho. Systolic Architecture for Vector Quantization. In *Vector Quantization*, H. Abut, editor, pages 499–512, IEEE Press, New York, 1990, (reprinted journal article).
6. Peter R. Cappello. Processor-Time Minimal Systolic Arrays. Chapt. 3 in *Transformational Approaches to Systolic Design*, Graham M. Megson, editor, pp. 53–76, Chapman Hall, Sep. 1993.
7. Peter Cappello, Omer Egecioglu, and Chris Scheiman. Processor-Time-Optimal Systolic Arrays. In *Highly Parallel Computations*, M. P. Bekakos (ed.), Advances in High Performance Computing Series, pp. 237 - 270, WIT Press, UK, 2001.
8. Peter Cappello and Christopher James Coakley. A Development and Deployment Framework for Distributed Branch-and-Bound. *To appear in Approximation Algorithms and Metaheuristics*, T. Gonzalez (ed.), CRC Press.

SOFTWARE

1. Javelin 1.0, 2002.
2. CX 1.0, 2003.
3. Jicos 1.0, 2004.

PATENTS

“Systolic super summation device,” Peter Cappello on behalf of the University of California and the National Science Foundation, and Willard L. Miranker on behalf of the IBM Corporation. European patent 87101193.8-, Feb. 10, 1987. US patent 4,751,665, June 14, 1988.

PRESENTATIONS

This is a list of presentations *other than those given at a conference with a published proceedings*. For presentations with multiple authors, the presentation was given by the author whose name is *italicized*.

1. (*Invited*) Peter Cappello. Unifying Systolic Design with Linear Transformations of Spacetime. Electrical Engineering-Systems Department Seminar, University of Southern California, Los Angeles, Feb. 1983.
2. (*Invited*) Peter Cappello. Unifying Systolic Design with Linear Transformations of Spacetime. Office of Naval Research Workshop on VLSI Architectures for Special-purpose Machines, Mt. Ada Conference Center, Catalina, CA, Mar. 1984.
3. (*Invited*) Peter Cappello. Mapping Gaussian Elimination onto Multiprocessor Architectures. Computer Science Department, Yale University, New Haven, CT, Aug. 1985.
4. (*Invited*) Peter Cappello. Systolic Design for Digital Signal Processing. Symposium on the Impact of VLSI on Signal Processing, Communications Research Laboratory, McMaster University, Hamilton, Ontario, CANADA, Oct. 1985.

5. (*Selected*) Peter Cappello. Solving Dense Linear Systems on a Hypercube Automaton. SIAM Conf. on Parallel Processing for Scientific Computing, Norfolk, VA, Nov. 1985.
6. (*Invited*) Peter Cappello. An FIR Filter Tissue. Office of Naval Research Workshop on Ultra Submicron Architectures, Pasadena, Dec. 1985.
7. (*Invited*) Peter Cappello. Systolic Design for Digital Signal Processing. IEEE Philadelphia Section Seminar on Systolic Parallel Architectures for Signal Processing, University of Pennsylvania, Apr. 1986.
8. (*Invited*) Peter Cappello. Languages and Tools for Systolic Computation. Office of Naval Research Workshop on Systolic Algorithms and Architectures, Hilton Head, SC, Dec. 1986.
9. (*Invited*) Peter Cappello. Representing Systolic Computation. Dept. of Electrical Engineering, UCLA, Nov. 1987.
10. Peter Cappello. A New Bijection between Natural Numbers and Rooted Trees. 4th SIAM Conf. on Discrete Mathematics, San Francisco, June 1988. (<http://www.cs.ucsb.edu/cappello/papers/1988SiamDM.html>)
11. (*Invited*) Peter Cappello. A VLSI layout for a Dadda Multiplier. Computer Engineering Seminar, University of Southern California, Los Angeles, March 1989.
12. Peter Cappello and Cetin K. Koc. Decomposing Chinese remaindering for systolic arrays. SIAM Ann. Meeting, San Diego, July 1989.
13. Peter Cappello, Cetin K. Koc, and Efstratios Gallopoulos. Systolic computation of interpolating polynomials. SIAM Conf. on Parallel Processing for Scientific Computing, Chicago, Dec. 1989.
14. (*Invited*) Peter Cappello. A Processor-Time Minimal Systolic Array for Matrix Product. Computer Science Colloquium, University of Oregon, Eugene, Apr. 1990.
15. Yoav Yaacoby and Peter Cappello. Decoupling the dimensions of a system of affine recurrence equations. The 6th Haifa Matrix Theory Conference, The Technion, Haifa, ISRAEL, June 1990.
16. Omer Egecioglu and Peter Cappello. A Bijection with Applications to Asymptotic Properties of Rooted Trees. 6th SIAM Conf. on Discrete Mathematics, Vancouver, BC, June 1992.
17. (*Invited*) Peter Cappello and Chris Scheiman. A Period-Processor-Time-Minimal Schedule for Cubical Mesh Algorithms. Electrical and Computer Engineering Seminar, Oregon State University, Corvallis, OR, Feb. 1993.
18. (*Invited*) Peter Cappello. Javelin: Internet-Based Parallel Computing Using Java. National Tsing Hua University (NTHU), Hsinchu, TAIWAN, April, 1998.
19. (*Invited*) Peter Cappello. Processor Lower Bound Formulas for Array Computations and Parametric Diophantine Systems. National Tsing Hua University (NTHU), Hsinchu, TAIWAN, April, 1998.
20. (*Invited*) Peter Cappello. Javelin: Internet-Based Parallel Computing Using Java.
21. (*Invited*) Peter Cappello. Javelin: Internet-Based Parallel Computing Using Java. National Taiwan University (NTU), Taipei, TAIWAN, April, 1998.
22. (*Invited*) Peter Cappello. Java-Based Parallel Computing on the Internet: Javelin 2.0 & Beyond. Seminar on High Performance Computing and Java, International Conference and Research Center for Computer Science, Schloss Dagstuhl, GERMANY, Aug. 2000.

23. (*Invited*) Peter Cappello. General Purpose Processors as Processor Arrays. IEEE 17th Int. Conf. on Application Specific Systems, Architectures, and Processors (ASAP), Steamboat Springs, CO, 2006.

PROFESSIONAL SERVICE

JOURNAL

Editorial Board

IEEE Transactions on Acoustics, Speech, and Signal Processing, '88 – '90.
Journal of VLSI Signal Processing, '88 – present.

Referee

Acta Informatica
Advances in Computing Research
Automatica
BIT
Computing
IEE Proc. (G) Circuits, Devices and Systems
IEEE Journal of Solid-State Circuits
IEEE Proceedings IEEE Trans. Circuits and Systems
IEEE Trans. Computers
IEEE Trans. Parallel and Distributed Systems
IEEE Trans. Signal Processing
Information Sciences
International Journal of Computer Aided VLSI Design
International Journal of Parallel Programming
International Journal of Science and Technology
Journal of Parallel and Distributed Computing
Journal of VLSI Signal Processing
Parallel Computing
Parallel Processing Letters

FUNDING ORGANIZATION

Member

NSF Review Panel for Research Initiation Awards, (Microelectronic Information Processing Systems Division), Washington.

Reviewer

Louisiana Board of Regents
MICRO
National Research Council (ARO)
National Science Foundation

CONFERENCE

Workshop Chair

IEEE Workshop on VLSI Signal Processing, USC, Los Angeles, '84.

Conference Co-Chair

IEEE Int. Conference on Application Specific Array Processors, Strasbourg, FRANCE, '95.

Technical Program Co-Chair

IEEE Int. Conference on Application Specific Array Processors, San Francisco, '94.

Program Committee Member

19th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, Cambridge, MA, Nov. 2007.

IEEE 18th Int. Conf. on Application Specific Systems, Architectures, and Processors (ASAP), Montreal, CANADA, Jul. 2007.

18th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, Dallas, TX, Nov. 2006.

IEEE 17th Int. Conf. on Application Specific Systems, Architectures, and Processors (ASAP), Steamboat Springs, CO, 2006.

17th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, Phoenix, AZ, Nov. 2005.

IEEE 16th Int. Conf. on Application Specific Systems, Architectures, and Processors (ASAP), Samos, Greece, July 23-25, 2005.

16th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, MIT, Cambridge, MA, Nov. 2004.

Int. Conf. on Application Specific Array Processors (ASAP), Galveston, Texas, September 27-29, 2004.

15th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, Marina Del Rey, CA, Nov. 2003.

Int. Conf. on Application Specific Array Processors, the Netherlands, June 24-26, 2003.

ACM Java Grande - ISCOPE Conference, Seattle, WA, 2002.

Int. Conf. on Internet Computing, Las Vegas, NV, 2002.

14th IASTED Int. Conf. on Parallel and Distributed Computing and Systems - PDCS, MIT, Nov. 2002.

Int. Conf. on Application Specific Array Processors, San Jose, CA, July, 2002.

PA Java 2001, Manchester, UK 2001.

- Int. Conf. on Application Specific Array Processors, Boston, MA 2000.
- Int. Conf. on Application Specific Array Processors, Geneva, SWITZERLAND, ITALY '97.
- Int. Conf. on Application Specific Array Processors, Chicago '96.
- IEEE Symposium on Parallel and Distributed Processing, Dallas, Dec. '95.
- IEEE Int. Conf. on Computer Design (Algorithms and Architecture track), Cambridge, MA '93.
- Int. Conf. on Application Specific Array Processors, Venice, ITALY '93.
- IEEE Workshop on VLSI Signal Processing, Koningshof, Veldhoven, The NETHERLANDS, '93.
- IEEE Int. Conf. on Computer Design (Algorithms and Architecture track), Cambridge, MA '92.
- Int. Conf. on Application-Specific Array Processors, Berkeley, '92.
- IEEE Workshop on VLSI Signal Processing, Napa Valley, CA, '92.
- IEEE Int. Conf. on Computer Design (Algorithms and Architecture track), Cambridge, MA '91.
- Int. Conf. on Application-Specific Array Processors, Barcelona, SPAIN, '91.
- IEEE Workshop on VLSI Signal Processing, San Diego, '90.
- Int. Conf. on Application-Specific Array Processors, Princeton, '90.
- Int. Conf. on Systolic Arrays, Killarney, IRELAND, '89.
- IEEE Workshop on VLSI Signal Processing, Monterey, '88.
- IEEE Workshop on VLSI Signal Processing, USC, Los Angeles, '86.

Session Chair

- “Cluster Computing,” IASTED Int. Conf. on Parallel and Distributed Computing and Systems, Phoenix, 2005.
- “Web Services & Tools,” IASTED Int. Conf. on Parallel and Distributed Computing and Systems, San Diego, 2003.
- Joint ACM Java Grande - ISCOPE (Int. Symp. on Computing in Object-Oriented Parallel Environments), Seattle, Nov, 2002.
- ‘Computer Arithmetic’, Int. Conf. on Application Specific Array Processors (ASAP), San Jose, CA, 2002.
- ‘Web Servers’, International Workshop on Scalable Web Services, Toronto, CANADA, 2000.
- ‘Efficient Design Methods I,’ Int. Conf. on Application Specific Array Processors, Venice, ITALY '93.
- ‘Short Presentations’, IEEE Workshop on VLSI Signal Processing, Napa Valley, CA '92.
- ‘Parallel Architecture,’ Int. Conf. on Application Specific Array Processors, Oakland, CA '92.

- 'Computer Arithmetic,' IEEE Int. Conf. on Computer Design, Cambridge, MA '91.
- 'Algorithms,' IEEE Workshop on VLSI Signal Processing, San Diego, '90.
- 'Bit-Level Systolic Systems,' Int. Conf. Systolic Arrays, Killarney, IRELAND, '89.
- 'Systolic Array Design,' IEEE Workshop on VLSI Signal Processing, Monterey, '88.
- 'Array and Parallel Processing,' 20th Ann. Asilomar Conf. Signals, Systems, and Computers, Pacific Grove, '86.
- 'Digital Signal Processing Theory I,' IEEE Workshop on VLSI Signal Processing, USC, Los Angeles, '86.
- 'Systolic Arrays,' Int. Conf. Acoustics, Speech, and Signal Processing, San Diego, '84.

SOCIETY

Chair

IEEE Signal Processing Society, Technical Committee on VLSI, '83 – '85 (Founding Chair), currently the TC Design and Implementation of Signal Processing Systems (DISPS).

Member

- Association for Computing Machinery (ACM)
- Senior member, Institute of Electrical and Electronics Engineers (IEEE):
 - Computer Society
 - Advisory Board, Signal Processing Society TC on DISPS.
- Upsilon Pi Epsilon

TEACHING

Computer Programming
Programming Methods
Foundations of Computer Science
Programming Project
Graph Algorithms
Automata and Formal Languages
Theory of Computation