NEW DSPs FOR NEXT GENERATION MOBILE COMMUNICATIONS

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Abstract — The implementation of new wireless communication standards often requires the design of new hardware capable of processing special algorithms. One approach of tackling the problem is the usage of dedicated hardware, optimized towards the corresponding algorithm, together with a DSP. However this may cause overhead in data transfers (DSP < - > ASIC) and requires additional control hardware and memories. The full design process including simulation and debugging of the whole system can be very time consuming. In this paper we avoid such problems by utilization of a new concept for application tailored DSPs. The architecture supports scaling and the inherent flexibility allows for the adaption to new algorithms. Examples such as equalization and the future wireless W-CDMA standard UMTS has been used to prove the applicability of the structure. In addition, the time-to-market factor can be significantly reduced.

1 Introduction

The nature of the mobile communication environment requires the connection of very different signal processing algorithms, operating at different clock speeds and with different demands in terms of precision and real-time capability. The classic approach of a system on a chip (SOC) comprises an embedded DSP core and dedicated parallel hardware on one die together with memories and controllers. This results in additional data transfers between DSP core and surrounding hardware. To support the introduction of a new wireless standard with increased signal processing complexity requires a new design of dedicated hardware, e.g. the equalizer structure or the channel-(de)coding scheme with new parallel hardware, separate memories and controllers.

In this paper we solve the problem by using a DSP architecture [1] which supports parallelism and is both scalable and extendable with dedicated datapaths. An efficient Instruction Set Architecture (ISA) allows for such customizations without changing large parts of the chip. Two different examples have been investigated as case studies for the new concept:

1) A classical single-carrier transmission system using a reduced-state-decision feedback MAP equalizer combined with a convolutional decoder (which can also be used for Viterbi or MAP decoding)

2) The W-CDMA RAKE receiver for the UMTS standard including the turbo decoding process.

First the DSP concept is shortly explained. Sections 3 and 4 give a short description of the algorithm problem and consider the impact upon the datapath design.

2 Concept for Application Tailored Signal Processors (CATS)

The concept was first presented in [1] and [2]. It is a research project at the Mannesmann Mobilfunk Chair. The above mentioned problems lead to the main goals:

- One processor family as the base for designing general purpose processors as well as application tailored (domain specific) processor types
- One processor development platform
- One generic software development platform, i.e. assembler, compiler, debugger which is independent on the tailorization
- A real-time development/debugging environment for the customer
- A uniform instruction set architecture which satisfies the statements above --- "TVLIW" [3]

In Figure 1 a simplified block schematic is shown. The

![Diagram](http://example.com/diagram.png)

Figure 1: CATS approach
dark gray marked blocks are not dependable on the application, while the datapaths change in number and functionality according to the specific application. The data memory (bandwidth) can be subject to customization as explained later on. The challenge of the concept is the reuse of as many functional units as possible while allowing for extendability, scalability and tailoring. This requires knowledge about the interactions of hardware/architecture and software/algorithm respectively. One fundamental paradigm follows: The functionality of a DSP can be orthogonalized into data transfer and data manipulation. Data transfer includes tasks such as data moves/loads, and all processing done in the program control unit, since transfers to/from program counter are performed. In contrast the actual algorithm execution is referred to as data manipulation. While the latter changes with the application all units belonging to data transfer should be fixed. In order to achieve full performance the orthogonalization must be represented in the Instruction Set Architecture (ISA) as well. A DSP’s ISA is a key issue since it fulfills the important task of bridging between software (flexibility) and hardware (complexity).

A new approach referred to as Tagged Very Long Instruction Word architecture (TVLIW) was developed [3]. It supports parallelism while keeping the code size at a reasonable amount. In the technique in-line and in-loop code is treated differently by dynamic assembly of the very long instruction word (VLIW). The overhead generated by composing the VLIW is most often hidden in the data flow pipeline. This is especially the case for dual-bus architectures, i.e. the memory bandwidth is limited to 2 accesses per cycle. This fact should be explained in more detail.

Turning back to the algorithm level we differ between matrix-vector operations such as shuffling algorithms (FFT, DCT, etc.), and vector-scalar operations (e.g. FIR, correlation), since they require different memory bandwidth when parallelism is applied. The latter can be considered as a class of sliding window algorithms, where a coefficient window slides over the data vector. Coefficient sharing over multiple multiply-accumulate datapath units (DPUs) leads to an constant memory bandwidth for highly parallel computation. An example is the block FIR where \( y_k = \sum_i x_k - a_i \) is calculated in parallel to \( y_{k+1} = \sum_i x_{k+1} - a_i \) and so forth. The coefficients \( a_i \) are the same in each datapath, while datapath unit \( n \) (DPUn) uses the x-value from datapath unit \( n-1 \) delayed by one cycle. The technique is also referred to as Zurich Zip. So it will take \( n \) cycles to feed \( n \) DPUs with data and the same time to update the according sections of the VLIW.

In this paper we assume the dual-access paradigm, i.e. only two busses broadcast the data to all units (see Fig. 2). The counterpart, the wide data memory approach was chosen in a different project for a HiPerLAN Modem DSP [4], where FFT-like operations are heavily utilized. Two examples should show the applicability of the architecture for new algorithms.

### 3 Combined Equalization and Decoding

The multipath propagation property of the mobile communication channel causes severe intersymbol interference (ISI), which comes along with fast time variations due to fading. Thus, data transmission in the presence of ISI asks for receivers which perform both, equalization and channel decoding. Different solutions have been proposed for soft-output equalizer techniques (e.g. SOVA [6]), which are known to be superior to hard-decision techniques. An interesting approach was presented by Koch and Baier [7], which should be used throughout this section. We will not reproduce the whole derivation, however the fundamental assumptions and equations will be given.

**Equalizer Structure & Implementation**

Starting with a simplified channel model (shift register process with memory \( L \)) an algorithm was derived which is a symbol-by-symbol based maximum probability estimator. It is similar to the one referred to as BCJR [8] or MAP (maximum-a-posteriori probability). Instead of probabilities their negative logarithm will be used. This simplifies the computation and enables fixed-point implementation. Furthermore, an approximation is introduced which avoids the calculation of logarithm and exponential leading to a group of equations, also known from the MAX-Log MAP [9]. The forward and backward state metrics \( A_f(S_k) \) and \( A_b(S_k) \) of state \( S \) at time \( k \) in the trellis are recursively calculated.

\[
A_f(S_k) = \min(A_f(S'_{k-1}) + \lambda(S'_{k-1}, S_k))
\]

\[
A_b(S_k) = \min(A_b(S'_{k+1}) + \lambda(S'_{k+1}, S_k))
\]

where in (1) the preceding states \( S'_{k-1} \) and \( S'_{k+1} \) are
defined by $S_k$ and $x_{k-L} = +1$ or $-1^1$. For the backward case (2) the $x_k = +1$ or $-1$ defines the selection. The branch metrics for the transition from state $S_{k-1}$ to $S_k$ are given by the distance calculation

$$\lambda(S_{k-1}, S_k) = |z_k - \sum_{i=0}^{L} x_{k-i}h_i|^2$$  \hspace{1cm} (3)

The soft-output value for bit $x_{k-L}$ is now defined by

$$q(x_{k-L}) = \min_{S_k | x_{k-L} = +1} (\lambda_f(S_{k-1}) + \lambda(S_{k-1}, S_k) + \lambda_f(S_k))$$

$$- \min_{S_k | x_{k-L} = -1} (\lambda_f(S_{k-1}) + \lambda(S_{k-1}, S_k) + \lambda_f(S_k))$$  \hspace{1cm} (4)

Fig. 3 shows the contributions to the $\min$-operation in both terms in equation (4) for $L = 2$.

Due to the soft-decision output the Koch & Baier equalizer outperforms its Viterbi counterpart by about 2 dB. However this benefit is dearly paid by an increase in computational complexity and a trippling in memory requirements due to the necessary storage of the backward metrics. It was found that the influence of the backward recursion is rather small. Assuming an influence depth of the $A_k(k)$ of only $L$ stages and all $A_k(k+L)$ are equally probable (typical initialization for backward recursion) the backward recursion can be implemented within the forward recursion [10]. Koch and Baier already took advantage from this fact which can be seen from equation (4), where the decision is made for $x_{k-L}$ using trellis states up to $S_k$, hence input values up to $x_k$ are used. Now the number of operations is of the same order as for the Viterbi Algorithm (VA).

In the previous section the trellis had $2^L$ states, thus the computation grows exponentially with the increase in channel influence length $L$. Reducing the number of states can significantly reduce the computational complexity. The performance loss is limited by a state-dependent feedback of hard decisions. The resulting derivative will be called Reduced-State-Decision Feedback (Bahl) Equalizer. The overall performance of such an approach is adequate for most of the channel types as simulations have shown [7].

The basic operations of this equalizer can be mapped to the functional units known from the classical VA. Hence we can distinguish between transition metric unit (TMU), add-compare-select unit (ACSU) and survivor path unit (SPU). The most complex operation takes place in the ACSU for which acceleration techniques are known. However, the computation of the transition metrics is now much more complex. It involves an FIR-like computation (see equation (3)) and depends upon the decisions made in the ACSU and stored in the SPU. Since we need a survivor path for each state for the reduced-state decision feedback, the back trace algorithm used in some DSPs is not applicable for our case. Instead we use a register exchange approach. The implementation is shown in Fig. 4. The SPU-hardware actual consists of $2^N$ 16-bit registers which can be divided into low and high byte, each half representing one bank of the register file. In normal mode the registers are available to the program control unit of the DSP for scratch-pad purposes. The additional hardware reduces to the controller and one-bit shift circuitry.

The datapath of the DSP itself is customized in a way that the ALU does not only support a 'SPLIT' mode allowing for parallel computations of two 16-bit values instead of one double precision 32-bit value. It also comprises an additional comparison unit in series, i.e. the Add-Compare-Select operation is performed in one machine cycle. Another feature accelerates the transmission metric update. Since the data for the FIR filter computation corresponds now to the survivors in the SPU and $x_k \epsilon \{ +1, -1 \}$, the multiplication reduces to a conditional accumulation (+ or -) of the complex channel coefficients. Thus the ALU has special inputs which conditionally control the internal Adder (see Fig. 5).

The new hardware results in more than 60% savings for
the equalization part compared to standard DSPs. In processors with Viterbi accelerators (e.g., TI ‘Lead’) the transition metric update together with the survivor path exchange is still a rather complex calculation. In particular the decision feedback of the reduced-state Bahi equalizer nearly neutralizes any performance gain of the C54x or CARMEL which support only the standard VA with traceback functionality. The proposed architecture outperforms such approaches by a factor of 2.4 and 1.6 (CARMEL) respectively. Figure 7 shows the benchmark results with a standard single MAC DSP as 100% reference. The figure also indicates the performance increase gained by an extension to 4 datapath units (DPU).

4 The IMT2000 Modem

The new Universal Mobile Communication Standard (UMTS) is currently subject to standardization. In this paper we use the specifications from 3GPP and IMT2000 which are characterized by:

- Wideband CDMA with chiprate of 3.84 Mcps
- RAKE receiver with 8 fingers
- Symbolrates between 3840 to 7.5 ksp
- Dual mode channel coding: convolutional (K=9) and turbo coding, rate 1/2 or 1/3

A simple block diagram of a possible receiver is shown in Fig. 6. The further parts of this sections are focused on the RAKE-receiver only (gray shaded area), which consists of 8 RAKE-fingers, each running at a different delay and/or with a different code. Each finger performs despreading with a special PN code and early/late computation for synchronization purposes. The despreaded symbols are weighted with a precalculated channel coefficient (FIR filter operation). An algorithm investigation revealed that the despreading operation itself represents more than 60% of overall computation while the weighting filter requires another 17%.

Since despreading is the most complex part this could be implemented in dedicated hardware running at 4 MHz. The actual FIR part has a much lower frequency and can be accomplished in a tiny standard DSP. However a 4 MHz clock for submicron silicon is far below the feasible rate and decreases the silicon efficiency. Additional I/O-transfers between the DSP and the despreaders hardware lead to further loss in efficiency. The problem seems attractive to prove the capability of our DSP concept. The following requirements for a new DSP were extracted from the analysis of the despread task.

- enough data memory to store a whole time slot
- support 8 bit arithmetic/storage
- 4 input registers for UMTS datapath with integration of PN-code generators into DPU

The basic operation in the despreaders itself is the correlation of a complex data vector $s$ with the corresponding complex code vector $c$ of length $S$. Since the code has a range of $c_k \in\{\pm 1 \pm j\}$ the multiply/accumulate of the correlator reduces to a code-dependent addition/subtraction of the input data to the accumulation value. This fact has been taken into account by designing the UMTS-datapath (see Fig. 8).

5 Results

The new UMTS-specific datapath has been described in VHDL, simulated and synthesized with standard-cell libraries. It contains a modified 40-bit ALU, a PN-code generator (basically a 18-bit shift register with set/hold functions) and a few additional multiplexers for data storage (de)compression, i.e. a complex value consisting of two 16-bit parts will be compressed into a single 16-bit memory word before memory storage and will be decompressed within the DPU after memory read.

Interestingly, the ALU-modification matches with the features added for the Equalizer from section 3. Furthermore the special support of the BCJR algorithm enables turbo decoding, which is part of the FEC in the standard. The required soft-input/soft-output modules can be easily implemented within the DSP, however the exhaustive memory needs of the interleaver block has to be taken into account.
Figure 7: Benchmarks for reduced state equalization

Figure 8: Structure of UMTS datapath

The comparison to a standard ALU shows an area increase of only 7% for the logic part, while providing the extended functionality. As a result, the RAKE-receiver part could be implemented within a 4-datapath architecture (each DPU consists of the proposed ALU and a MAC). This corresponds to the capability of 1200 pure DPU-MOPS @100MHz and leads to the benchmarks given in Fig. 9. The total DSP core size is about 4 mm² in 0.25 μm 4-layer-metal technology.

6 Conclusions

A new architecture for high performance DSPs has been investigated in terms of its capacity to handle algorithms of future mobile communication standards. The modular system provides support for very complex tasks and can also be downscaled or extended according to the target application. Thus it is flexible enough to fulfill the tight requirements of today's communications sector by providing a uniform development platform on both the hardware and the software side.

References


