

Mohit Tiwari

Electrical Engineering and Computer Sciences
University of California, Berkeley
tiwari@eecs.berkeley.edu
(805) 708-4506
<http://www.eecs.berkeley.edu/~tiwari>

Research Interests

I am interested in designing computer architectures and systems with strong formal foundations. My thesis introduced gate-level information flow tracking (GLIFT), a technique that can provably track all digital information flows through full systems, and the Execution Lease architecture designed to explicitly support precise space-time sandboxes. In the longer term, I envision that *every* machine will be a high assurance system, even dynamic ones such as datacenters and smart-phones, and I want to research systems where the entire hardware-software stack lends itself to precise monitoring and run-time adaptation in order to meet formally specified objectives.

Education

Ph.D. in Computer Science University of California, Santa Barbara	September 2011 Santa Barbara, CA
M.S. in Computer Science University of California, Santa Barbara; GPA 3.96/4	June 2010 Santa Barbara, CA
Bachelor of Technology, Computer Science Indian Institute of Technology; GPA 8.95/10	May 2005 Guwahati, India

Honors and Awards

- **Computing Innovation Fellow**, with Prof. Krste Asanović and Prof. Dawn Song, University of California, Berkeley, 2011-12.
- **Outstanding Dissertation Award**, Department of Computer Science, University of California, Santa Barbara, 2011.
- **IEEE Micro Top Pick** Micro's Top Picks from Computer Architecture Conferences, January-February 2010.
- **Best Paper Award**, Parallel Architecture and Compiler Techniques (PACT), Sept 2009. Raleigh, NC.
- **Outstanding Teaching Assistant Award**, Department of Computer Science, UC Santa Barbara. March 2006.

Research Experience

User-centric Secure Systems University of California, Berkeley	8/2011 - present Berkeley, CA
---	--

Post-doctoral scholar mentored by Prof. Krste Asanović and Prof. Dawn Song. Our goal is a system that spans smart clients and datacenter servers, and allows end-users to intuitively control their private data while developers use an API to create secure programs. This requires co-designing user interfaces and application frameworks together with system software and hardware accelerators to yield a practical, secure system.

Information Flow Secure Architectures **6/2006 - 7/2011**
University of California, Santa Barbara **Santa Barbara, CA**
Research assistant (advisor: Prof. Timothy Sherwood) working primarily on architectures and program analyses for security and software reliability. Other projects include using thermo-electric coolers (TECs) to reduce datacenter cooling costs, and a language for designing secure hardware.

3D-Integrated Hardware for Trustworthy Systems **8/2009 - 9/2009**
Naval Postgraduate School **Monterey, CA**
Visiting Researcher (host: Prof. Theodore Huffmire). Worked jointly with Prof. Cynthia Irvine and Dr. Timothy Levin on using 3D-ICs to create trustworthy systems.

Systems for Many Core Processors **6/2007 - 8/2007**
NEC Laboratories **Princeton, NJ**
Summer Intern (advisor: Dr. Hari Cadambi). Worked jointly with Dr. Anand Raghunathan on scaling map-reduce to many-core processors.

Application-Specific SRAMs for Embedded Systems **6/2004 - 8/2004**
EDA Group, Politecnico di Torino **Torino, Italy**
Summer Intern (advisor: Prof. Enrico Macii). Worked jointly with Prof. Luca Benini on implementing an SRAM generator that automatically optimizes SRAM block sizes based on the memory access pattern of an embedded application.

Teaching and Work Experience

Post-doctoral Fellow **8/2011 - Current**
University of California, Berkeley **Berkeley, CA**
Research in privacy-preserving applications and architectures and mentoring graduate students.

Teaching Assistant **9/2005 - 5/2006**
University of California, Santa Barbara **Santa Barbara, CA**
Graduate Computer Architecture, Undergraduate Operating Systems and Introduction to Programming courses: responsible for labs and discussion sections.

Programmer **5/2005 - 8/2005**
Headstrong Services India **Bangalore, India**
Implementing a distributed cache using Internet Communications Engine (ICE) for a stock exchange server.

Summer Intern **5/2003 - 8/2003**
Center for Development of Advanced Computing (CDAC) **Trivandrum, India**
Implementing a USB 2.0 device controller in Verilog HDL.

Publications

Crafting a Usable Microkernel, Processor, and I/O System with Strict and Provable Information Flow Security Mohit Tiwari, Jason Oberg, Xun Li, Jonathan K Valamehr, Ben Hardekopf, Ryan Kastner, Frederic T Chong, and Timothy Sherwood. *in Proceedings of the International Symposium of Computer Architecture (ISCA), June 2011. San Jose, CA*

Fighting Fire with Fire: Modeling the Data Center Scale Effects of Targeted Superlattice Thermal Management Susmit Biswas, Mohit Tiwari, Luke Theogarajan, Timothy Sherwood, and Frederic T Chong. *in Proceedings of the International Symposium of Computer Architecture (ISCA), June 2011. San Jose, CA*

Caisson: A Hardware Description Language for Secure Information Flow, Xun Li, Mohit Tiwari, Jason Oberg, Frederic T Chong, Timothy Sherwood, and Ben Hardekopf, *in Proceedings of the ACM Conference on Programming Language Design and Implementation (PLDI). June 2011. San Jose, CA.*

Information Flow Isolation in I2C and USB, Jason Oberg, Wei Hu, Ali Irturk, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, *in Proceedings of the Design Automation Conference (DAC). June 2011. San Diego, CA.*

Theoretical Fundamentals of Gate Level Information Flow Tracking, Wei Hu, Jason Oberg, Ali Irturk, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (in press).*

Hardware Assistance for Trustworthy Systems through 3-D Integration, Jonathan Valamehr, Mohit Tiwari, Timothy Sherwood, Ryan Kastner, Ted Huffmire, Cynthia Irvine, and Timothy Levin, *in Annual Computer Security Applications Conference (ACSAC), December 2010. Austin, TX.*

Theoretical Analysis of Gate Level Information Flow Tracking, Jason Oberg, Wei Hu, Ali Irturk, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, *in Proceedings of the 47th Design Automation Conference (DAC), June 2010. Anaheim, CA.*

Tracking Information Flow at the Gate-Level for Secure Architectures, Mohit Tiwari, Xun Li, Hassan Wassel, Bitu Mazloom, Shashidhar Mysore, Frederic Chong, and Timothy Sherwood, *in IEEE Micro: Micro's Top Picks from Computer Architecture Conferences, January-February 2010.*

Execution Leases: A Hardware-Supported Mechanism for Enforcing Strong Non-Interference, Mohit Tiwari, Xun Li, Hassan M G Wassel, Frederic T Chong, and Timothy Sherwood, *in Proceedings of the International Symposium on Microarchitecture (MICRO), December 2009. New York, NY.*

Quantifying the Potential for Program Analysis Peripherals, Mohit Tiwari, Shashidhar Mysore, and Timothy Sherwood, *in Proceedings of Parallel Architecture and Compiler Techniques (PACT), September 2009. Raleigh, NC [Best Paper Award].*

Complete Information Flow Tracking from the Gates Up, Mohit Tiwari, Hassan

Wassel, Bitu Mazloom, Shashidhar Mysore, Frederic Chong, and Timothy Sherwood, *in Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2009. Washington, DC.

A Small Cache of Large Ranges: Hardware Methods for Efficiently Searching, Storing, and Updating Big Dataflow Tags, Mohit Tiwari, Banit Agrawal, Shashidhar Mysore, Jonathan K Valamehr, and Timothy Sherwood, *in Proceedings of the International Symposium on Microarchitecture (MICRO)*, November 2008. Lake Como, Italy.

Workshop Papers

Hardware Trust Implications of 3-D Integration Ted Huffmire, Timothy Levin, Michael Bilzor, Cynthia Irvine, Jonathan Valamehr, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, *Workshop on Embedded Systems Security (WESS) October 2010. Scottsdale, Arizona*

Secure Information Flow Analysis for Hardware Design: Using the Right Abstraction for the Job, Xun Li, Mohit Tiwari, Ben Hardekopf, Timothy Sherwood, Frederic Chong, *in Proceedings of the Fifth ACM SIGPLAN Workshop on Programming Languages and Analysis for Security (PLAS) June 2010, Toronto, Canada*

Function Flattening for Lease-Based, Information-Leak-Free Systems, Xun Li, Mohit Tiwari, Timothy Sherwood, and Frederic Chong, *Poster at the 21st IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), July 2010, Rennes, France*

MadMAC: Building a Reconfigurable Radio Testbed Using Commodity 802.11 Hardware, Ashish Sharma, Mohit Tiwari, and Haitao Zheng, *IEEE Workshop on Networking Technologies for Software Defined Radio (SDR) Networks, 2006, Reston, VA.*

Professional Activities

Reviewer for conferences and journals: International Symposium of Computer Architecture (ISCA), Parallel Architectures and Compilation Techniques (PACT), Code Optimization and Generation (CGO), Transactions on Architecture and Code Optimization (TACO), IEEE International Symposium on Workload Characterization (IISWC), Annual Computer Security Applications Conference (ACSAC).

Program Committee member for the Computer Science Department's Graduate Student Workshop on Computing (GSWC), 2007 and 2008.

References

Prof. Timothy Sherwood
Associate Professor
Department of Computer Science
University of California, Santa Barbara
Office 1119, Harold Frank Hall

Santa Barbara, CA 93106-5110
<http://www.cs.ucsb.edu/~sherwood/>
Email: sherwood@cs.ucsb.edu
Phone: 805-448-9362

Prof. Frederic T Chong

Professor
Department of Computer Science
University of California, Santa Barbara
Office 5163, Harold Frank Hall
Santa Barbara, CA 93106-5110
<http://www.cs.ucsb.edu/~chong/>
Email: chong@cs.ucsb.edu
Phone: 805-310-7931

Prof. Ryan Kastner

Associate Professor
Department of Computer Science and Engineering
University of California, San Diego
9500 Gilman Drive, Mail Code 0404
La Jolla, CA 92093-0404
<http://cseweb.ucsd.edu/~kastner/>
Email: kastner@cs.ucsb.edu
Phone: 805-350-0049

Prof. Dawn Song

Associate Professor
Computer Science Division
University of California, Berkeley
675 Soda Hall
Berkeley, CA 94720-1776
<http://www.cs.berkeley.edu/dawnsong/>
Email: dawnsong.letters@cs.berkeley.edu
Phone: 510-642-8282

Prof. Krste Asanović

Associate Professor
Computer Science Division, EECS Department
The Parallel Computing Laboratory
University of California at Berkeley
579 Soda Hall
Berkeley, CA 94720-1776
Email: krste@eecs.berkeley.edu
Phone: 510-642-6506