

# SimGate: Full-System, Cycle-Accurate Simulation of the Stargate Intermediate Node for Sensor Networks\*

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## Abstract

*We present an accuracy and performance analysis of SimGate – a full-system simulation of the Stargate intermediate-level, resource-constrained, sensor network device. We also examine ensemble simulations using SimGate and either one or two simulated Mica2 Motes using the same criteria. We find that accurate functional behavior and cycle counts (at the full device level) are achievable using SimGate alone, and in conjunction with simulated Motes. Also, the slowdown compared to real-time for these simulations is modest with respect to previously published work.*

## 1 Introduction

Sensor networks have emerged as a technology for transparently interconnecting our physical world with more powerful computational environments, and ultimately, global information systems. In a typical sensor network, computationally simple, low-power sensor elements take physical readings and may perform some processing of these readings before ultimately relaying them to more powerful computational elements. The need for non-intrusiveness motivates sensor design toward small, inexpensive, low-power sensor implementations that can be deployed in large numbers throughout the environment to be sensed. Because the sensor elements themselves are so resource constrained, however, a sensor network must include a smaller number of more complex and general purpose computational elements that are capable of substantial in-network processing, contain greater storage capacity, and can act as a “gateway” between the network of sensor

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elements and more power-intensive network technologies.

Designing and investigating these ensemble systems, to date, has relied primarily on physical deployments and experimentation [8, 13, 14, 20, 32]. While the quality of the results from such efforts is excellent, the need to work with the physical systems directly imposes a substantial research impediment. The labor cost, equipment cost, space requirements, debugging complexity, etc., that characterize such an engineering-based approach, all limit the scope of the research that can be performed, and the number of researchers who can perform it.

One obvious possibility for widening the scope of what can be investigated is to employ simulation as a complement to experimentation with deployed systems. While several simulation efforts have focused on the sensing elements themselves [17, 22, 23, 26, 28, 29], an approach that combines sensor simulation with simulations of the other “heavier” devices as an ensemble – and does so with an acceptable level of accuracy – is necessary to make simulation a viable option.

In this paper, we investigate SimGate – a full-system simulation of the Intel Stargate device [27] (distributed by Crossbow Inc.) – that we have developed for use with sensor element simulations as part of a simulated ensemble. The Stargate device is intended to function as a general purpose processing, storage, and network gateway element in a sensor network deployment. These devices are battery powered, and are both fewer in number and larger in size than the sensing devices. The Stargate’s more intrusive nature facilitates the use of large batteries that enable longer battery life and improved compute and storage capability.

Our goal is to provide both functional correctness and cycle-count accuracy at the device level, in a simulation of the Stargate that can be coupled with simulated sensors. The currently available tools for simulating more complicated, heavy-weight, intermediate sensor nodes (such as the Stargate) are limited. For example, there are tools for simulation of the Intel XScale processor [34] and its power consumption [4, 7] alone. However, to our knowledge, there are no simulation tools that simulate the complete Stargate device.

SimGate captures the behavior of the Stargate internal components including the processor, memory hierarchy, communications (serial and radio), and peripherals. In essence, SimGate is

a *virtual device*, in that it boots and runs the Familiar Linux operating system and any program binary that executes over it, *without modification*. SimGate is also able to accurately estimate processor cycle counts. Moreover, this functionality can be toggled to trade off cycle-accuracy for simulation performance.

We are also able to couple SimGate with our own simulations of the Crossbow Mica2 sensor nodes (called SimMote ) to produce a simulated sensor network *ensemble*. These simulations are also virtualized representations of the physical hardware (i.e. full-system emulations providing accurate cycle counts). SimMote provides similar functionality to that of existing Mote simulation and emulation systems [17, 22, 23, 26, 28, 29]. We make no claims as to its superiority over these systems – instead, we have used SimMote to expedite our investigation and empirical evaluation of heterogeneous device, ensemble simulation.

To empirically evaluate the efficacy of our system, we measure the accuracy (in terms of Stargate machine cycles) and real-time performance of SimGate using a range of stressmarks and community benchmarks. We also present results for similar experiments in which the SimGate and SimMote interoperate via a serial interface (simulated in both). Finally, we examine three-device ensemble consisting of a SimGate node, a serially-connected SimMote, and a third SimMote that communicates only via simulated radio. For these latter two cases, we run our own multi-device benchmark suite. Each experiment compares simulated results to measurements gathered empirically from physical Stargate and/or Mica2 devices. In all cases throughout this study, the actual hardware devices and simulations run the same operating system and benchmark binary, without modification. Thus, the results test the degree to which our simulations may be used in place of physical hardware in each experimental setting.

Our results indicate that we are able to accurately simulate the full system of an intermediate Stargate node with a *maximum error* of 12.4% across all benchmarks we test. We also find that, on average, simulation at this level of accuracy imposes a slowdown of  $58X$  over real-time device execution and that a slowdown of  $20X$  can be achieved if only a functional simulation (i.e. without accurate cycle counts) is required. As a result, we believe this work demonstrates the potential of

multi-device, sensor network simulation as a research-enabling technology.

In the next section, we overview the design and implementation of our simulator. In Section 3, we describe our experimental setup and measurement methodology. We then detail the accuracy and performance of our system in Section 4. In Sections 5 and 6, we present related work and conclude with some observations and our plans for future work respectively.

## **2 SimGate Simulator**

Simulation is a potentially an important tool for sensor network system and application development. The focus of most prior work in system simulation has been on high-end, general-purpose, wall-powered devices [25, 18, 19], processor and power simulation [1, 34, 4, 7], or on the sensing devices themselves [17, 22, 23, 26, 28, 29]. However, to our knowledge, no extant approach to sensor network simulation enables full-system simulation of a key sensor network component, the intermediate “gateway” node. Moreover, no simulation system facilitates co-simulation of different sensor network devices as part of an ensemble. The goal of our work is to investigate, implement, and evaluate such techniques.

Intermediate nodes are resource-constrained, battery-powered, devices that provide a bridge between sensor nodes (which we refer to as Motes after the popular Berkeley Mote implementation [16]) and more powerful, wall-powered, computational environments. Intermediate nodes are commonly responsible for sensor device control and in-network processing [15] of sensor data: receiving, processing, assimilating, forwarding, etc. These nodes reduce the power consumption of the system by reducing the communication distance from the Motes to a powered device, and by coalescing and compressing the data that is forwarded to higher levels of the hierarchy. Intermediate nodes commonly have longer battery life and significantly more powerful computation and communication capabilities than the Motes. A popular example of an intermediate node implementation is the Intel Stargate [27].

To simulate intermediate nodes, we developed a software system, called SimGate, that virtualizes the Stargate device. SimGate emulates the complete functionality of the Stargate and pro-

vides cycle-accurate simulation of the Stargate’s Intel XScale processor pipeline [35]. SimGate is completely transparent to the above software layers – i.e., the system boots and executes the popular embedded OS, Handhelds.org Familiar Linux and any program that executes over it, without modification. Moreover, SimGate eases sensor network program development by implementing a unified debugging interface. In this section, we present the design and implementation of the SimGate architecture.

## 2.1 SimGate Design and Implementation

SimGate provides full-system simulation of the Stargate intermediate sensor node. The Stargate is a single-board, embedded system (designed by Intel Research) that is comprised of a 400MHz Intel XScale processor, an Intel SA1111 companion chip for I/O, Intel StrataFlash, SDRAM, PCMCIA/CF slots, and serial connector for a Mote [27]. Currently, the Stargate design does not include a radio interface that is compatible with Motes. Instead, the Stargate implements an expansion bus that allows a Mote to be physically attached to it. In *situ*, the Stargate communicates with Motes in a sensor network via a Mote that is physically connected to it via this bus.

The goal of our design and implementation of SimGate is to effectively trade-off simulator overhead for accuracy while enabling transparent, full-system simulation. To this end, we combine a number of different approaches to performance estimation of device components within a single system, including cycle-level simulation of some components (which can be disabled when only functional simulation is needed) and benchmark-based timing. For both functional and cycle-accurate simulation, SimGate executes the same operating system and application binary as the actual device.

We simulate the following features of the Stargate device:

- ARM v5TE instruction set without Thumb support and with XScale DSP instructions
- XScale pipeline simulation, including the 32-entry TLBs, 128-entry BTB, 32KB caches and 8-entry fill/write buffers
- PXA255 processor, including MMU (co-processor), GPIO, interrupt controller, real time clock, OS timer, and memory controller
- Serial device (UART) that communicates with the attached Mote

- SA1111 StrongARM companion chip
- 64MB SDRAM chip
- 32MB Intel StrataFlash chip
- Orinoco wireless LAN PC card including the PCMCIA interface

We do not simulate the 802.11b radio model or the Stargate battery, i.e. SimGate is not power-accurate. We do simulate the serial interface that enables SimGate to communicate with the attached Mote (or a simulated Mote). The support of this set of Stargate components is sufficient to enable us to successfully boot the Linux kernel 2.4.19 and to execute a wide range of Stargate benchmarks.

To implement the instruction set, we use a simple interpreter to execute the instruction flow using a large switch statement as is done in SimpleScalar [1]. The most complex part of the CPU core simulation is the memory management unit (MMU). The MMU is used constantly during program execution since each memory access requires an address translation. When cycle-level simulation is not required, we turn off simulation of the individual MMU components including the TLB, BTB, I/D caches, and fill/write buffers, to improve functional simulation performance. The cycle-level simulation of these components do not affect the correctness of functional program execution but they do, however, impose a large simulation cost. To further improve the address translation speed, we have implemented an address lookup cache (soft TLB) for both instruction and data addresses. This soft TLB increases functional simulation time by 10% on average.

To achieve the cycle accuracy of processor core simulation, we have implemented a simulation component for the XScale CPU pipeline. The Intel XScale core employs a seven or eight stage (depending on the instruction flow), single-issue, super pipeline. There are three pipelines that execute in parallel after the execution stage. As a result, multiplication and memory access can happen concurrently and results may be written back to memory out of order.

Since we were unable to obtain publically available documentation from Intel on the pipeline logic, we have based our implementation on the pipeline implementation in the XTREM power simulator [7]. We have used this implementation as a reference and extended and evolved it using

benchmark measurements from a real Stargate device (since the Stargate implements a slightly different version of XScale processor than that implemented within XTREM). We have implemented the MMU components (TLB, BTB, caches and buffers) within our pipeline simulator. Since these components are transparent to data correctness, we only perform fast symbolic simulation without the actual data movement. To account for cache and TLB miss penalties, the simulator uses estimates that we obtained via measurements from hand-coded benchmark execution on a real device.

We toggle cycle-level simulation through the use of a special virtual hardware interface that we integrated into the XScale hardware performance monitor (HPM) interface. When any software activates and terminates HPMs, the simulator turns pipeline simulation on and off, respectively. We have selected this implementation since it enables us to use the same interface to drive experimentation and measurement of programs executed with either unsimulated (real device) or simulated configurations easily.

To support such toggling, our pipeline simulation is trace-based. That is, after an instruction is executed using functional simulation, we feed it to the pipeline simulator to drive the clock. This may result in a delay between the execution and the clock advance. This delay is on the order of several cycles on average; as a result it has very little impact on the device level cycle accuracy (which we report in Section 4).

The most important peripheral and I/O devices that we simulate are the Flash chip and the Orinoco PCMCIA wireless card. The Flash chip is controlled by memory mapped I/O registers. The simulator sends and receives I/O commands and data through these registers. In the Flash chip, a state machine controls the sequence of operations. We simulate both the interface and the internal state machine according to a Verilog model of the Flash chip from Intel (<http://www.intel.com/design/flcomp/toolbrfs/298189.htm>). The simulation of the wireless card consists of two parts: the PCMCIA interface and the wireless card interface. We have implemented the former using publically available interface. The latter is not publically available and as such, we simulate the card by mimicking card interface exposed in the Linux driver source code and using the parameters dumped from the real card.

We do not maintain cycle accuracy of the I/O devices (whether cycle-accurate simulation is turned on or off) due to the device-specific complexities and widely ranging functionality. Instead we employ a similar benchmarking approach to the one discussed previously to estimate the performance of I/O devices. That is, we collect the timing behavior using a range of hand-coded benchmark experiments, and use this data to advance the clock within the simulator.

## **2.2 Coupling SimGate with Other Sensor Network Simulators**

To explore simulation of SimGate with that of other sensor network components, we have developed a simulation of the Crossbow Mica2 Mote, called SimMote. We emphasize that SimMote is intended to provide similar functionality to other Mote simulators [29, 30, 23, 17, 22, 28] and as such, we make no claim as to its relative scientific value. Implementing SimMote simply has ensured, in the most expedient way, that the Mote simulation is interoperable with, and comparable to, SimGate.

Mica2 features the 8MHz Atmel ATmega128 microcontroller (simple 16-bit RISC ISA), on-board Flash memory and a 900MHz radio. Compared to SimGate, the SimMote is much easier to implement given the significantly simpler hardware and software design (it also has the added benefit of testing the flexibility of our simulation development framework).

SimMote currently supports the following features:

- AVR instruction set
- Most on-chip functions: program memory, IO registers, timer, serial device (UART), interrupts, SPI (Serial Peripheral Interface), and ADC (Analog/Digital Converter)
- 512KB on-board flash
- Serial ID chip
- CC1000 radio chip
- Simple radio transmission model (described below)

We achieve cycle accuracy of the AVR ISA for most instructions since the instruction set specifies fixed cycle counts. We use these timings within SimMote to forward the CPU clock. In a way anal-

ogous to SimGate, SimMote is able to boot the TinyOS operating system and to execute existing Mote programs.

To couple device simulators, we have developed a multi-simulation manager. The manager is a multi-threaded software system that controls the life cycle of constituent simulators, e.g., it provides simulator services that include create, start, stop, join and leave. The manager forks a thread for each simulator invokes the start routine in each. The start routine initiates the OS boot process and uses a configuration file to invoke the benchmark or set of benchmarks of interest. The manager also implements a unified debugging interface (which we describe below) that dispatches debug commands to different simulators.

To achieve cycle-accurate, coordinated simulation of multiple simulators, the proportion of the rates of execution of simulated devices must be held to be roughly the same as that for real devices. This coordination is important for execution as well as for communication (e.g., for a radio or serial connection). To enable this coordination, we employ a simple, lock-step method that forces the clock within each simulator to synchronize periodically. This is similar to the synchronization mechanism in the Avrora Mote simulator [29], however, we maintain separate, individual clocks per simulator as opposed to a single global clock.

To implement this synchronization, the multi-simulation manager inserts a synchronization event into the event queue of each simulator when each is first instantiated. The event repeatedly fires at a fixed interval. When the event fires, all of the threads of simulation meet at the same clock point before continuing execution. We set the synchronization interval based on the clock frequency of the communication technologies. Since the fastest technology is serial transmission between the Mote and the Stargate (at 57.6KB/second), we use the one byte serial transmission time as the synchronization period. This equals 128 Mote cycles.

We have implemented a simple Mote radio model within SimMote based on the model implemented in Avrora [29]. Our model is different in that we do not use a global clock across simulators or a centralized packet dispatching/assembly object. Instead, we distribute each transmitted packet to the receiving device simulator which assembles the packet locally, using its own clock. Since

the simulators execute in lock step, our choice of a 128 Mote cycles synchronization period is sufficient to cover radio transmission, i.e., correct packet assembly, which requires 19.2KB/s.

Since the clock rate of a Stargate is 54 times that of a Mote, we must synchronize SimGate simulators with SimMote simulators. To enable this, we can use a SimGate synchronization interval that is 54 times that of the SimMote. An interesting side effect of this however, is that doing so forces us to simulate the Motes *as slow as* the Stargate. Since the machine on which we run our simulations is much faster than the real speed of the Mote, we can simulate up to 6 times faster than real Mote execution. However, in an ensemble system of heterogeneous device simulators, the fastest machine simulated is the performance bottleneck. As such, we must slow the SimMotes to match SimGate speed.

### **2.3 Other Simulation Framework Features**

Debugging is a key component in an ensemble system of sensor network devices simulators. To facilitate debugging, we have implemented a unified debugging interface and dispatch within the multi-simulation manager that supports debugging of concurrently executing simulation systems.

The manager dynamically dispatches debug commands to the individual simulators. Since each simulator runs on a separate thread, the debugger can attach to any of the simulator threads to control its execution flow and to watch the change in the execution state. The functions we support in the simulators include step execution, the dump of memory and flash, and watching of internal state and break points.

Another useful function that we have implemented is checkpointing. Our checkpointing mechanism within each simulator saves the current, full-system, simulation state including the snapshot of memory and flash file system. We provide mechanisms that facilitate the storage and loading of such images to enable fast forwarding and continuation of an executing system.

## **3 Experimental Method**

To evaluate and analyze the performance and accuracy of SimGate, we performed a number of experiments with the SimGate alone and with SimGate-SimMote ensembles. To evaluate the latter,

Benchmark	Executables	Description
adpcm	adpcmdecode/adpcmencode	Adaptive differential pulse code modulation for audio coding
g721	g721decode/g721encode	CCITT voice compression
gsm	gsmencode/gsmdecode	European standard for speed coding
jpeg	jpegenencode/jpegdecode	Lossy compression for still images

**Table 1. MediaBench benchmarks that we used in the evaluation of SimGate.**

we implemented two scenarios: (1) A Mote attached to a Stargate through the expansion bus; and (2) A secondary Mote communicating with the first via simulated radio. Scenario (1) represents the use of the Stargate as a gateway.

Scenario (2) represents a sensor network that has one Mote and one gateway (a Stargate with a Mote attached). In this scenario, the serially-connected Mote and Stargate act as a packet forwarding engine to and from the sensor network. In this scenario, we set the Mote antennae to be in physical contact to minimize errors caused by interference. At present, we do not model interference as part of the simple radio model that we implement, however, we are currently working on robust and accurate radio models as part of future work.

In the following subsections, we first detail the benchmarks that we use for the SimGate alone and for our ensemble scenarios. We also describe the experimental apparatus that we use to collect our simulated and actual measurements.

### 3.1 Benchmarks

For stand-alone SimGate evaluation, we employed hand-coded “stressmarks” and benchmarks from the suites of both MiBench [12] and Mediabench [5]. Due to space constraints, we only include the results from Mediabench in this paper; our technical report version of this paper contains all of the data [31]. Table 1 describes the benchmarks from Mediabench. We eliminate three benchmarks due to the constraints of the underlying platform: *Epic* does not run on the real Stargate platform (due to memory constraints), *MPEG2* requires too many hours to execute due to the execution of floating point operations, and *Ghostscript* does not fit in the available Stargate Flash memory (25MBytes). We execute all remaining benchmarks from the RAM drive.

Benchmark	Description	Functional Unit
Ping	Echoes network packet back to sender	Network interface
Sense	Processes a sensor read query	Analog/Digital converter
APS [21]	Ad-hoc positioning system (heavy FP computation)	Arithmetic/Logic unit
Log	Reads log from Flash	Secondary Flash & UART
Multi	Parallel APS computations on both Mote and Stargate	Arithmetic/Logic unit

**Table 2. Benchmarks that we used to evaluate the ensemble simulation of SimGate and SimMote. The third column shows the functional units that are exercised most heavily during benchmark execution.**

To evaluate ensemble simulation, we employ open-source applications as well as hand-coded programs. We describe the applications in Table 2. Column 3 shows the functional units of the Motes that are heavily utilized during the execution of various benchmarks. In choosing benchmarks, we attempt to exercise the full device, and cover the major functions of a Mote: communication, sensing, and logging.

Each ensemble benchmark has a *Long* and *Short* form. The Short benchmarks exercise only the Stargate and serially-attached Mote communicating via the UART interface (scenario 1). The Long benchmarks exercise the Stargate and the attached Mote operating together as a gateway or controller, and a remote Mote communicating via radio (scenario 2). Moreover, each of these applications (except the Multi benchmarks) takes the form of a remote procedure call (RPC). When the program on the Stargate sends a query to the Mote, it blocks until the receiver completes the appropriate execution and returns. The Multi benchmark also tests concurrent computation by running parallel computations of ad-hoc positioning system (APS) [21] on both Mote and Stargate. This test is useful to evaluate the performance of simulating coordinated computation on Mote and Stargate.

### 3.2 Experimental Apparatus

We execute TinyOS v1.1 on the Motes (and SimMote ) and a variation of Familiar Linux v0.5.1 on the Stargate (and SimGate). For the stand-alone Stargate applications (i.e. Mediabench), we measured the CPU clock cycles and instruction count using the XScale hardware performance monitors (HPM).The HPM system can monitor three events (CPU clock cycles and two events)

Benchmark	$\mu_{meas}$	$\mu_{simulated}$	$\mu_{meas} - \mu_{simulated}$	% error $\pm$ 95% conf. bound
adpcmdecode	3.367E+07	3.069E+07	2.980E+06	8.9% $\pm$ 0.28%
adpcmencode	3.068E+07	2.766E+07	3.014E+06	9.8% $\pm$ 0.36%
g721decode	6.272E+08	5.735E+08	5.368E+07	8.6% $\pm$ 0.17%
g721encode	6.527E+08	6.006E+08	5.213E+07	7.9% $\pm$ 0.44%
gsmdecode	1.526E+08	1.420E+08	1.061E+07	7.0% $\pm$ 0.57%
gsmencode	4.335E+08	3.995E+08	3.401E+07	7.8% $\pm$ 0.09%
jpegdecode	2.554E+07	2.235E+07	3.191E+06	12.5% $\pm$ 1.16%
jpegencode	5.412E+07	4.731E+07	6.813E+06	12.5% $\pm$ 0.41%

**Table 3. SimGate accuracy results. The table presents average cycle counts for measurements and simulations of MediaBench benchmarks, the 95% confidence interval on the difference between the means, and the fraction of the average measurement that the interval constitutes.**

concurrently. We read the performance monitors using a kernel module that we developed.

We ran our simulators on a dedicated Linux (kernel ver 2.6.8) machine. The machine has a 64bit AMD Opteron CPU running at 2.4GHz and 4GB of memory. To measure wall clock execution time of each benchmark, we modified the simulator. Each time the performance monitoring registers of the simulated machine (i.e. Stargate) are accessed, the simulator reads the real (wall-clock) time from the host system (which is synchronized using NTP), and computes and logs the delta (time since previous access).

We *wrap* each simulated application using a small program: The wrapper reads the HPMs immediately before and after the execution of simulated program. This enables us to collect both wall clock time and simulator statistics (number of instructions executed, number of clock cycles, and many other system events supported by XScale architecture).

## 4 Results

We detail the accuracy of SimGate by comparing it to the Stargate in terms of the number of cycles required to execute the benchmarks described in the previous section. In the first set of comparisons, we make 20 identical runs of each benchmark on both SimGate and Stargate and compare the average number of cycles required per benchmark.

Table 3 gives the result of this comparison in the following format. The first column shows the name of the benchmark, the second column ( $\mu_{meas}$ ) shows the average number of cycles measured

on the Stargate hardware, the third column ( $\mu_{simulated}$ ) presents the cycles reported by SimGate, and the fourth column shows the difference. In the fifth column, we report the error percentage ( $|(\mu_{meas} - \mu_{simulated})/\mu_{meas}|$ ) which is difference between the average of the measured cycle counts and the average of those generated by the simulator. We also compute the 95% confidence interval for the error percentage using a Student  $t$  distribution [9] with 19 degrees of freedom to model the difference of the averages (marked as  $\pm$  confidence bound in the table).

Note that the error percentage and confidence interval also indicate whether we should reject the null hypothesis of equivalence in a two-sided hypothesis test at 95% confidence. If the “margin for error” (confidence interval) spans 0% (i.e. the margin is greater than the error percentage itself), we fail to reject the null hypothesis of equivalence and hence cannot determine whether the observed difference in averages is due to random variation or not. In this experiment, however, the confidence intervals are all quite narrow indicating the error percentage we observe for each benchmark is statistically significant at the 95% confidence level.

We observe that the accuracy of SimGate for this set of benchmarks is acceptable as a full-system simulation. While error percentages below 5% have been achieved for individual system components [7, 1], because we simulate the full device (including all parts of the memory hierarchy and the interrupt structure) and run both an operating system and application on it, we expect to introduce additional error. That the maximum error is no more than 13.5% (with 95% confidence) and most of the errors are below 10%, is surprising and is an indication that the simulation is of high quality.

#### 4.1 Coupled SimGate and SimMote Simulations

To gauge how well SimGate will work in a simulation of a heterogeneous sensor network, we examine its cycle-count accuracy when it is used in conjunction with one or two SimMotes (as described in Section 3). Table 4 shows the cycle count results for the benchmarks that exercise the Stargate device and the Mote that is connected to it via a serial interface (scenario 1). As noted previously, the Stargate device does not support a radio device capable of communicating directly with Motes in a sensor network. Instead, it uses Mote directly connected to it via a serial interface

Benchmark	$\mu_{meas}$	$\mu_{simulated}$	$\mu_{meas} - \mu_{simulated}$	% error $\pm$ 95% conf. bound
PingShort	9.414299E+07	9.592680E+07	-1.783813E+06	1.9% $\pm$ 6.6%
SenseShort	2.040608E+08	2.051871E+08	-1.126267E+06	0.6% $\pm$ 1.1%
APSShort	1.997744E+08	1.966910E+08	3.083427E+06	1.5% $\pm$ 0.07%
MultiShort	2.128019E+08	2.080650E+08	4.736897E+06	2.2% $\pm$ 1.5%
LogShort	1.637669E+08	1.695956E+08	-5.828771E+06	3.6% $\pm$ 1.25%

**Table 4. Scenario 1 accuracy results. The table shows the average cycle counts for measurement and simulation of the benchmarks coupling SimGate with simulated Mote via serial link. The final column shows the error percentage for a 95% confidence bound.**

as a network interface peripheral. These benchmarks are intended to exercise this interaction in a representative way.

The format of Table 4 is the same as that described for Table 3 in the previous subsection. Again, the sample size used to calculate each average is 20 and we compute a 95% confidence interval on the error percentage using a  $t$  distribution with 19 degrees of freedom.

Again, the accuracy of the coupled simulation is reasonable for two communicating independent full-device simulations. Note that while the error percentages appear significantly lower than for the SimGate simulation alone, the confidence intervals are also significantly wider. Thus, based on error percentage alone it may appear that the coupled simulations are more accurate. However, there is more relative variation (as we might expect) in the coupled case. As a result, it is the error range, and not the specific error value, that is significant in this case.

For example, consider the results for the *PingShort* benchmark shown in row 1 of Table 4. From the data, it is not possible to determine that the difference between the measured average and simulated average is statistically significant at the 95% confidence level (since the error range spans 0%). However, there is enough variation in both measurements and simulation to make the difference indistinguishable from random variation across an interval that is  $\pm 6.6\%$  centered on the observed average.

The *PingShort* benchmark exhibits the widest variation, as indicated by the error range. For the *SenseShort* benchmark the difference in observed average is, once again, statistically undetectable with 95% confidence, but the error range is smaller. In the remaining three cases, there is a sta-

Benchmark	$\mu_{meas}$	$\mu_{simulated}$	$\mu_{meas} - \mu_{simulated}$	% error $\pm$ 95% conf. bound
PingLong	3.228130E+08	3.116003E+08	1.121275E+07	3.5% $\pm$ 2.9%
SenseLong	2.267467E+08	2.254300E+08	1.316726E+06	0.58% $\pm$ 2.1%
APSLong	2.273877E+08	2.212660E+08	6.121661E+06	2.7% $\pm$ 6.3%
MultiLong	2.362925E+08	2.285356E+08	7.756869E+06	3.3% $\pm$ 3.3%
LogLong	1.891255E+08	1.915953E+08	-2.469811E+06	1.3% $\pm$ 2.4%

**Table 5. Scenario 2 accuracy results. The table shows the average cycle counts for measurement and simulation of the benchmarks coupling SimGate with simulated Mote via serial link communicating with a Mote via the radio. The final column shows the error percentage for a 95% confidence bound.**

tistically significant difference, but both the error percentages and the confidence bounds on those percentages are remarkably small. From this data, we conclude that cycle-counts taken from SimGate when coupled to SimMote via a serial interface, while introducing additional variation, are still reasonably accurate.

The final set of accuracy results we present is for benchmarks that couple SimGate with a SimMote via its serial interface that is then used to communicate with a second SimMote via the radio interface (scenario 2). As described previously, we do not yet know of a Mote radio communication simulation that is accurate enough not to overshadow the accuracy (or lack thereof) of SimGate. Thus, these experiments reflect a configuration in which the antenna of the two Motes are in physical contact. It is our experience that this configuration eliminates much of the variation resulting from radio communication.

Table 5 depicts these results using the same format as the in the previous two tables. Similar to the results for *PingShort* and *SenseShort* in Table 4, the additional variation introduced by the second Mote and the radio communication makes the difference between observed and simulated averages indistinguishable from random variation at a 95% confidence level. However, the 95% confidence intervals on the error percentage are, once again, similar in magnitude to the error percentages in Tables 3 and 4 for the cases where the averages are significantly different.

From all three tables, then, we conclude that SimGate achieves a similar level of accuracy both when it is used as a single device simulation, and when it is part of a multi-device simulation in which the devices are communicating. Because the software, including the operating system, run

Benchmark	$t_{meas}$	$t_{nocycle}$	$t_{cycle}$	$r_{nocycle}$	$r_{cycle}$
adpcmdecode	7.60E-2	1.05E+00	3.23E+00	13.84	42.50
adpcmencode	8.40E-2	1.21E-02	3.61E+00	14.34	42.97
g721decode	1.57E+00	3.70E+01	1.13E+02	23.51	71.73
g721encode	1.64E+00	4.19E+01	1.19E+02	25.45	72.39
gsmdecode	3.82E-01	1.06E+01	2.86E+01	27.65	74.79
gsmencode	1.09E+00	3.01E+01	8.54E+01	27.67	78.64
jpegdecode	6.31E-02	7.28E-01	2.37E+00	11.54	37.61
jpegencode	1.35E-01	2.02E+00	6.18E+00	14.95	45.85

**Table 6. SimGate execution performance.** The table presents the average execution time (in seconds) for measurement (meas) and simulation (w/cycle accuracy disabled (nocycle) and enabled versions (cycle)) of the MediaBench benchmarks. The final two columns show the slowdown for cycle-accurate simulation and functional simulation, respectively.

by the physical hardware in each of these three experiments is precisely the same as that executed by the simulated devices, we believe that SimGate can be used as an effective tool for estimating Stargate cycle counts in heterogeneous sensor network configurations.

## 4.2 SimGate Execution Performance

Since our ultimate goal is to provide a complete sensor network simulation capability that can be used to complement current deployment-based research strategies, the real-time slowdown of SimGate versus the physical hardware is an important consideration. Table 6 compares wall-clock timings of the Stargate device to SimGate ( $t_{cycle}$ ) and to SimGate with the cycle-accuracy features disabled ( $t_{nocycle}$ ). For cases where cycle accuracy is desired, we can enable the parts of SimGate that are necessary to make cycle count estimates internally. Comparing the performance of the resulting functional simulator to the full SimGate simulation gives the cost of achieving the accuracy levels described previously.

The simulator is 10 to 27 times slower than the real hardware when cycle accuracy is not required. This factor is smallest for adpcm and jpeg (approximately 10 times) and higher for gsm and g741 (approximately 25 times). Cycle accurate simulation ( $r_{cycle}$ ) increases the cost by 2.93X (37 to 78 times slower than real hardware). There is a higher variance in these numbers, e.g., gsm vs jpeg, than for functional simulation ( $r_{nocycle}$ ). One reason for this is cycle-accurate cache sim-

ulation. The *time required to simulate a cache miss and a cache hit is the same* – although the simulator adjusts the simulated clock and cycle counts appropriately for each. On a real device a cache hit is much faster than a cache miss. Thus, application memory access patterns can have a large effect on the relative slow down of simulation. We are encouraged by these results since other full system, cycle-accurate, simulations of advanced computer systems executing an OS and application, e.g., SimOS, report slowdowns of  $4000X$  –  $6000X$  [25] although the results are not completely comparable since we use different host machines and simulate different targets.

## 5 Related Work

There is a large body of research on simulation systems. In this section, we identify techniques that are most similar to our work. In particular, we describe and contrast frameworks for ensemble simulation for devices relevant to a sensor network and for tools for full system emulation.

### 5.1 Frameworks for Ensemble Sensor Network Simulation

There have been a number of significant efforts to simulate and emulate sensor network devices. Most of this prior work has focused on the sensing devices and in particular Mote devices. These projects include Simulavr [26], ATEMU [23], Mule [30] Avrora [29], TOSSIM [17], SensorSim [22] and SENS [28]. Although, we implemented Mote simulation as part of this project, we did so only to investigate ensemble simulation system for SimGate. We could have alternatively coupled current approaches with SimGate but decided instead to implement our own Mote simulator to expedite the coupling process.

The ATEMU and Avrora Mote simulation platforms are most similar to our system. Both provide full-system multi-simulation of Mote devices. However, the multi-simulation enabled by these systems is *homogeneous* – only simulation of Mote devices are coupled and no other sensor network devices, e.g., intermediate nodes, are supported. Both systems use a lock-step method similar to ours to synchronize simulation threads and enable accurate timing and correct communication. ATEMU synchronizes at each cycle and Avrora loosens the synchronization period to thousands Mote cycles. Both ATEMU and Avrora can simulate Motes in real time. Since Avrora

is written in Java, its performance is highly dependent on JVM implementation. In our work, we use the similar synchronization technique as in Avrora. However, we must deal with more complex situation in which coordination between devices happens between very different devices. To simulate only Motes (as is done in these prior works), we achieve slightly better performance than Avrora because of the use of C++ instead of Java.

There are also systems that employ *heterogeneous*, ensemble simulation. In particular, our design vision is similar to the work described in [11]. This prior work describes a comprehensive framework that supports the simulation, emulation, and deployment of heterogeneous sensor network systems and applications. This framework uses TOSSIM [17] to emulate Motes and EmStar [10] to emulate “microservers” (a general term for platforms like Stargate). The authors employ a wrapper library, EmTOS, to glue the two simulation systems together by enabling the execution of Mote application on EmStar. In the framework, all applications must be re-compiled and linked to the specific library to be emulated by the system.

In SimGate, our goal is to enable the study, verification, debugging, and analysis of sensor network applications using a simulation platform that does not require any modification to the binaries of the applications or operating system on which they run. This enables increased flexibility for researchers and ensures that the simulation execution environment is the same as that on the real devices. This SimGate model also enables us to easily obtain important application characteristics (e.g. accurate cycle estimation and interrupt properties) that is more difficult to collect in an emulative environment. Emulation systems do have a speed advantage however. For example, TOSSIM [17] can emulate a Mote 50 times faster than actual Mote execution using a 1.8GHz Pentium IV machine. EmStar can execute re-compiled, microserver code at native speed. In SimGate, we enable users to toggle functional and cycle-accurate simulation to reduce the overhead of the latter. Moreover, we are currently investigating other optimization techniques to improve simulation speed while maintaining cycle accuracy.

## 5.2 Full System Simulation

From the perspective of full system simulation and emulation, there are number of software systems that support a wide range of devices [25, 34, 33, 18, 19, 2, 24, 3]. Once such, very popular, system is SimOS [25]. SimOS is a full system simulator containing simulation models for most common hardware components, e.g., processor, memory, disk, network interfaces, etc. SimOS features a range of advanced processor models that trade-off accuracy for simulation speed. The fastest model applies dynamic binary translation [6, 33] for maximal simulation speed. The finest-grain model simulates the advanced pipeline structure to provide accurate cycle-level behavior. SimOS is able to simulate the MIPS R4000 processor on a machine with the same architecture, with a slowdown of about  $10X$  for binary translation and  $5000X$  for detailed pipeline simulation on a SGI 4-processor (150MHz) machine.

SKYEYE ([www.skyeye.org](http://www.skyeye.org)) is a similar project that simulates a number of ARM-based processors and development boards. SKYEYE also emulates a number of peripherals, including LCD and the ethernet interface. SKYEYE is based on the GDB ARM emulator which naturally enables the use of gdb as a debugging interface – in much the same way that we do. Although some of the techniques employed in these projects are complementary and useful to our endeavor, these systems are not intended or used for sensor network research. The focus of our work is on a toolset for full-system emulation combined with cycle-accurate simulation of heterogeneous sensor network devices.

## 6 Conclusion

In an effort to make sensor network research more widely accessible and to ease sensor software development and evolution, we have developed a system for full-system, functional and cycle-accurate simulation of intermediate sensor nodes. Our system, called SimGate, implements the complete Intel Stargate device and executes the Linux operating system and XScale applications transparently, without modification.

We investigate the accuracy and efficiency of SimGate in isolation as well as in concert with sen-

sensor device (Mote) simulation. Our results indicate that SimGate is functionally correct and enables cycle accuracy (if desired) within 9% on average for the benchmarks that we evaluated. When we co-simulate SimGates with SimMotes (our Mote simulator), our system introduces accuracy error of less than 4% in all cases. On average, our system is 20X slower than a real device when using functional emulation and 58X slower when using cycle-accurate pipeline simulation. We believe that these results indicate that SimGate can be used as an effective tool for accurately simulating Stargate intermediate nodes in heterogeneous sensor network configurations. As part of future work, we plan to investigate techniques for accurate radio and battery modeling, optimization of simulation speed, the scalability of our multi-simulation system for large-scale sensor networks, and simulation of other devices and components.

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